HEF4043B

Quad R/S latch with 3-state outputs Rev. 13 — 8 December 2021

Product data sheet

1. General description

The HEF4043B is a quad R/S latch with 3-state outputs and common output enable input (OE). Each latch has set (nS), and reset (nR) inputs and a 3-state output (nQ). When OE is LOW, the latch outputs are in the high impedance OFF-state. OE does not affect the state of the latch. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD} .

2. Features and benefits

- Wide supply voltage range from 3.0 to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- · Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Specified from -40 °C to +85 °C

3. Applications

• Four-bit storage with output enable

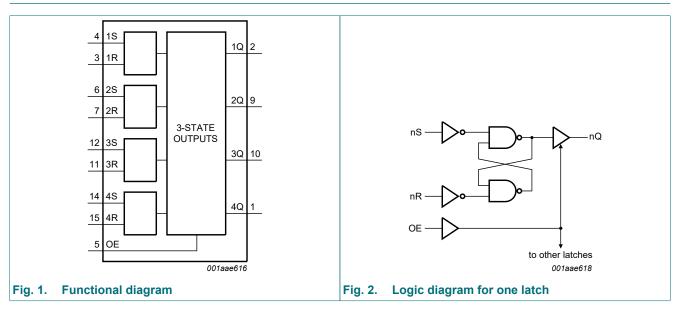
4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4043BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

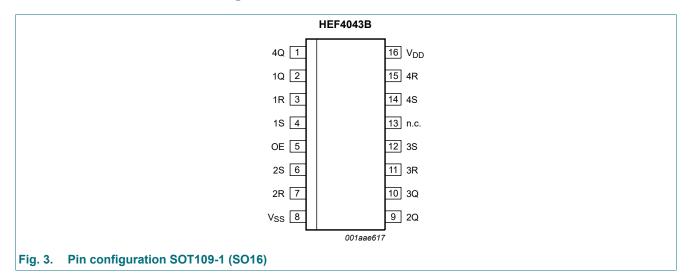


5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description							
Symbol	Pin	Description					
1Q, 2Q, 3Q, 4Q	2, 9, 10, 1	3-state buffered latch output					
1R, 2R, 3R, 4R	3, 7, 11, 15	reset input (active HIGH)					
1S, 2S, 3S, 4S	4, 6, 12, 14	set input (active HIGH)					
OE	5	common output enable input					
V _{SS}	8	ground supply voltage					
n.c.	13	not connected					
V _{DD}	16	supply voltage					

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance state.

Inputs	Output		
OE	nS	nR	nQ
L	Х	Х	Z
Н	L	Н	L
Н	Н	Х	Н
Н	L	L	latched

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	V_{I} < -0.5 V or V_{I} > V_{DD} + 0.5 V	-	±10	mA
VI	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm DD}$ + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T _{amb} -40 °C to +85 °C	-	500	mW
Р	power dissipation	per output	-	100	mW

9. Recommended operating conditions

Table 5. Red	able 5. Recommended operating conditions							
Symbol	Parameter	Conditions	Min	Тур	Мах	Unit		
V _{DD}	supply voltage		3	-	15	V		
VI	input voltage		0	-	V _{DD}	V		
T _{amb}	ambient temperature	in free air	-40	-	+85	°C		
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	-	3.75	μs/V		
		V _{DD} = 10 V	-	-	0.5	μs/V		
		V _{DD} = 15 V	-	-	0.08	μs/V		

10. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0 V$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} =	-40 °C	T _{amb} =	+25 °C	T _{amb} =	+85 °C	Unit
				Min	Max	Min	Max	Min	Мах	1
V _{IH}	HIGH-level input voltage	I ₀ < 1 μΑ	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	I ₀ < 1 μΑ	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	I ₀ < 1 μΑ	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level output voltage	I ₀ < 1 μΑ	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
l _l	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I _{OZ}	OFF-state output current	nQ output HIGH; returned to V _{DD}	15 V	-	1.6	-	1.6	-	12.0	μA
		nQ output LOW; returned to V_{SS}	15 V	-	1.6	-	1.6	-	12.0	μA
I _{DD}	supply current	I _O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
CI	input capacitance			-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

 V_{SS} = 0 V; T_{amb} = 25 °C unless otherwise specified; for waveforms and test circuit see <u>Section 11.1</u>.

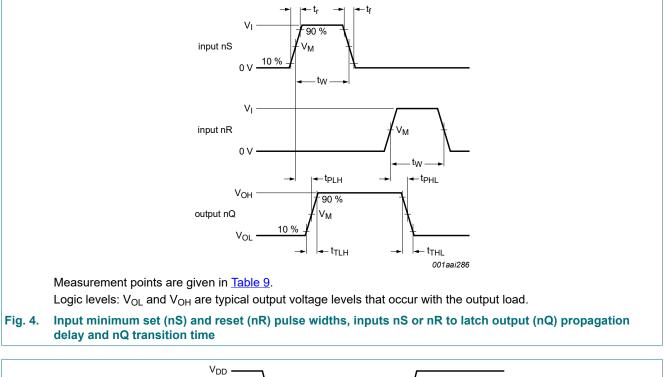
Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula [1]	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	$nR \rightarrow nQ;$	5 V	63 ns + (0.55 ns/pF)C _L	-	90	180	ns
	propagation delay	see <u>Fig. 4</u>	10 V	24 ns + (0.23 ns/pF)C _L	-	35	70	ns
			15 V	17 ns + (0.16 ns/pF)C _L	-	25	50	ns
t _{PLH}	LOW to HIGH	$nS \rightarrow nQ;$	5 V	38 ns + (0.55 ns/pF)C _L	-	65	135	ns
	propagation delay	see <u>Fig. 4</u>	10 V	14 ns + (0.23 ns/pF)C _L	-	25	50	ns
			15 V	7 ns + (0.16 ns/pF)C _L	-	15	35	ns
t _t	transition time	nQ output;	5 V [2]	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
		see <u>Fig. 4</u>	10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _{PHZ}	HIGH to OFF-state	$OE \rightarrow nQ;$	5 V		-	45	90	ns
	propagation delay	see <u>Fig. 5</u>	10 V		-	20	35	ns
			15 V		-	10	25	ns
t _{PLZ}	LOW to OFF-state	$OE \rightarrow nQ;$	5 V		-	50	100	ns
	propagation delay	see <u>Fig. 5</u>	10 V		-	20	40	ns
			15 V		-	10	25	ns
t _{PZH}	OFF-state to HIGH	$OE \rightarrow nQ;$	5 V		-	25	50	ns
	propagation delay	see <u>Fig. 5</u>	10 V		-	15	30	ns
			15 V		-	10	25	ns
t _{PZL}	OFF-state to LOW	$OE \rightarrow nQ;$	5 V		-	40	80	ns
	propagation delay	see <u>Fig. 5</u>	10 V		-	20	45	ns
			15 V		-	15	35	ns
t _W	pulse width	nS input HIGH;	5 V		30	15	-	ns
		see <u>Fig. 4</u>	10 V		20	10	-	ns
			15 V		16	8	-	ns
			5 V		30	15	-	ns
		minimum width; see <u>Fig. 4</u>	10 V		20	10	-	ns
		366 <u>Fiy. 4</u>	15 V		16	8	-	ns

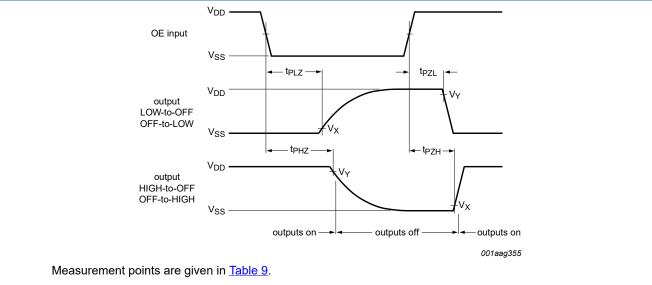
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF). [2] t_t is the same as t_{THL} and t_{TLH} .

Table 8. Dynamic power dissipation P_D

 P_D can be calculated from the formulas shown. $V_{SS} = 0$ V; $t_r = t_f \le 20$ ns; $T_{amb} = 25$ °C.

Symbol	Parameter	V _{DD}	Typical formula for P_D (μ W)	where:
P _D	dynamic power	5 V	$P_{D} = 1100 \text{ x } f_{i} + \Sigma (f_{o} \text{ x } C_{L}) \text{ x } V_{DD}^{2}$	f _i = input frequency in MHz;
	dissipation	10 V	$P_{D} = 4400 \text{ x f}_{i} + \Sigma(f_{o} \text{ x C}_{L}) \text{ x V}_{DD}^{2}$	$f_o = output frequency in MHz;CL = output load capacitance in pF;$
		15 V	P_D = 11400 x f _i + Σ(f _o x C _L) x V _{DD} ²	V_{DD} = supply voltage in V; $\Sigma(f_o \times C_L)$ = sum of the outputs.





11.1. Waveforms and test circuit

Fig. 5. Output enable (OE) to latch output (nQ) enable time (t_{PZL} and t_{PZH}) and disable time (t_{PLZ} and t_{PHZ})

Table 9. Measurement points

Supply voltage	Input		Output		
V _{DD}	V _I V _M		V _M V _X V _Y		V _Y
5 V to 15 V	V _{DD} or 0 V	0.5V _{DD}	0.5V _{DD}	0.1V _{DD}	0.9V _{DD}

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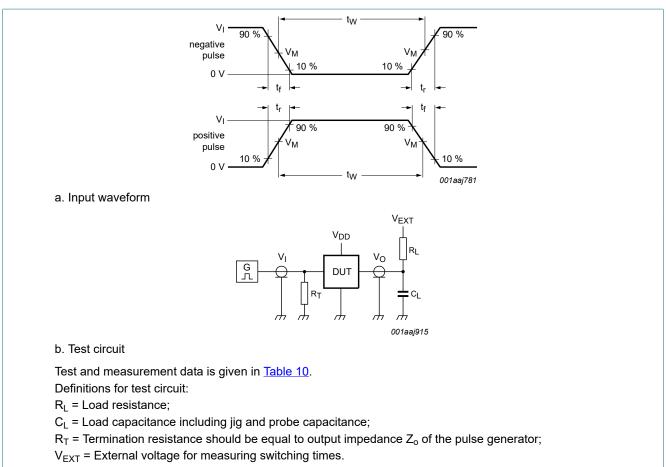


Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V _{EXT}		
V _{DD}	VI	t _r , t _f	CL	RL	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
5 V to 15 V	V _{DD}	≤ 20 ns	50 pF	1 kΩ	open	V _{DD}	GND

12. Package outline

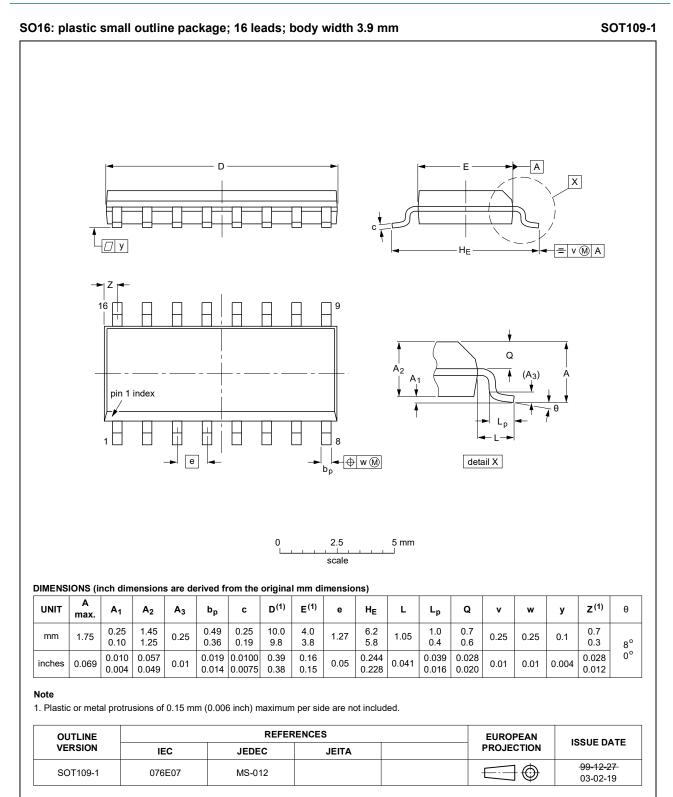


Fig. 7. Package outline SOT109-1 (SO16)

HEF4043B

13. Abbreviations

Table 11. Abbreviations					
Acronym	Description				
CMOS	Complementary Metal-Oxide Semiconductor				
DUT	Device Under Test				
ESD	ElectroStatic Discharge				
HBM	Human Body Model				
MM	Machine Model				

14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4043B v.13	20211208	Product data sheet	-	HEF4043B v.12
Modifications:	Section 1 and Section 13 add	d <u>Section 14</u> updated. dded.		
HEF4043B v.12	20200130	Product data sheet	-	HEF4043B v.11
Modifications:	Nexperia.	f this data sheet has been rede ave been adapted to the new c corrected.		
HEF4043B v.11	20160324	Product data sheet	-	HEF4043B v.10
Modifications:	Type number	HEF4043BP (SOT38-4) remov	/ed.	
HEF4043B v.10	20111118	Product data sheet	-	HEF4043B v.9
Modifications:	• <u>Table 6</u> : I _{OH} r	ninimum values changed to ma	iximum	- I
HEF4043B v.9	20091216	Product data sheet	-	HEF4043B v.8
HEF4043B v.8	20091127	Product data sheet	-	HEF4043B v.7
HEF4043B v.7	20090710	Product data sheet	-	HEF4043B v.6
HEF4043B v.6	20081111	Product data sheet	-	HEF4043B v.5
HEF4043B v.5	20080729	Product data sheet	-	HEF4043B v.4
HEF4043B v.4	20080710	Product data sheet	-	HEF4043B_CNV v.3
HEF4043B_CNV v.3	19950101	Product specification	-	HEF4043B_CNV v.2
HEF4043B_CNV v.2	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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