DACx3608 Octal, 10-Bit or 8-Bit, I²C Interface, Buffered Voltage Output DACs in Tiny 3 × 3 QFN Package

1 Features

- Ensured Monotonic
- Wide Operating Range
  - Power Supply: 1.8 V to 5.5 V
  - Temperature Range: –40˚C to 125˚C Wide Operating Range
- I²C-Compatible Serial Interface
  - Standard, Fast, and Fast+ Mode
  - 2.4-V, V_{IH} with V_{DD} = 5.5 V (no IOVDD needed)
- LDAC Pin For Simultaneous Output Update
- Very Low Power: 0.1 mA/Channel at 1.8 V
- Low Power Startup Mode: Power up to 10K-GND State
- Tiny Package
  - 16-Pin QFN (3 mm × 3 mm)

2 Applications

- Programmable Power Supplies
- VCOM Biasing in Display Panel
- Laser Driver In Multifunction Printers
- Auto Focus Digital Still Cameras Lens
- ATM Machines, Currency Counters, Barcode Readers
- IP Network Cameras, Projectors

3 Description

The DAC53608 and DAC43608 are a pin-compatible family of eight-channel, buffered voltage-output digital-to-analog converters (DACs) that have 10-bit and 8-bit resolution. The external reference range of 1.8 V to 5.5 V gives full scale output voltage of 1.8 V to 5.5 V. These devices are monotonic across the power supply range.

The devices communicate through the I²C interface. These devices support I²C standard mode (100 kbps), fast mode (400 kbps), and fast+ mode (1 Mbps). These devices have a load DAC (LDAC) pin that allows simultaneous DAC updates.

The DACx3608 devices have a power-on-reset circuit that makes sure the DAC registers start and stay at zero scale until a valid code is written to the registers.

The DACx3608 also includes per channel, user programmable, power down registers. These registers facilitates the DAC output buffers to start in a power down to 10K state and remain in this state until a power up command is issued to these output buffers.

The DACx3608 devices operate within the temperature range of –40°C to 125°C. The devices are available in a tiny QFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DAC53608	WQFN (16)	3.00 mm × 3.00 mm
DAC43608	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, refer to the orderable addendum at the end of the data sheet.

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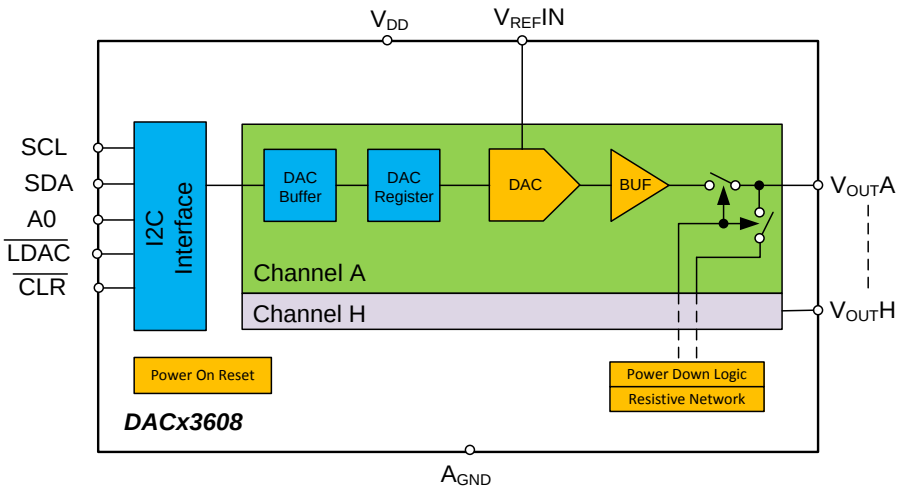
Simplified Block Diagram



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4 Revision History

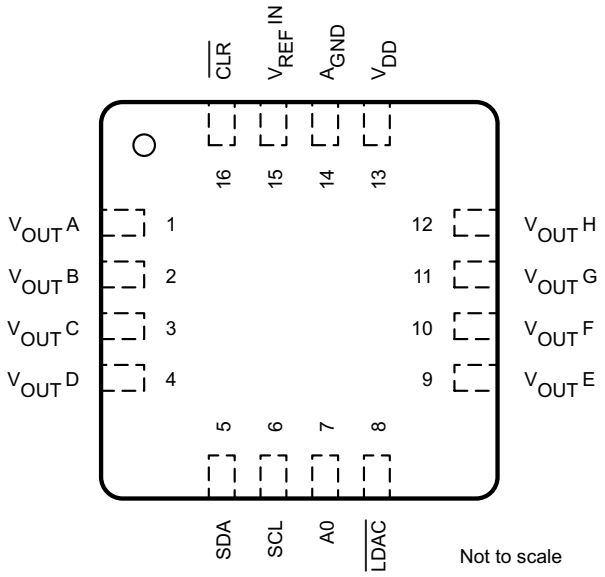
DATE	REVISION	NOTES
October 2018	*	Advance Information release.

5 Device Comparison Table

DEVICE	RESOLUTION
DAC53608	10-Bit
DAC43608	8-Bit

6 Pin Configurations and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$V_{OUT}A$	O	Analog output voltage from DAC A
2	$V_{OUT}B$	O	Analog output voltage from DAC B
3	$V_{OUT}C$	O	Analog output voltage from DAC C
4	$V_{OUT}D$	O	Analog output voltage from DAC D
5	SDA	I/O	Data is clocked into or out of the input register. This pin is a bidirectional, open - SDA drain data line that must be connected to the supply voltage with an external pull-up resistor.
6	SCL	I	Serial interface clock
7	A0	I	Four-state address input
8	$\overline{LDAC}$	I	Load DAC pin for simultaneous output update (active low)
9	$V_{OUT}E$	O	Analog output voltage from DAC E
10	$V_{OUT}F$	O	Analog output voltage from DAC F
11	$V_{OUT}G$	O	Analog output voltage from DAC G
12	$V_{OUT}H$	O	Analog output voltage from DAC H
13	V_{DD}	PWR	Analog supply voltage (1.8 V to 5.5 V).
14	A_{GND}	GND	Ground reference point for all circuitry on the device.
15	$V_{REF}IN$	I/O	Reference input to the device
16	$\overline{CLR}$	I	Asynchronous clear pin (active low)

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{DD} to A_{GND}	–0.3	6	V
Input voltage	V_{REF}IN to A_{GND}	–0.3	V_{DD}+0.3	V
Input voltage	Digital input(s) to A_{GND}	–0.3	V_{DD}+0.3	V
Output voltage	V_{OUT} to A_{GND}	–0.3	V_{DD}+0.3	V
Input Current	Current into any pin	–10	10	mA
Junction temperature range (TJ max)		–40	150	°C
Storage temperature, Tstg		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±1000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 500-V HBM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ±WWW V and/or ±XXX V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. [Following sentence optional; see the wiki.] Manufacturing with less than 250-V CDM is possible with the necessary precautions. [Following sentence optional; see the wiki.] Pins listed as ±YYY V and/or ±ZZZ V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to A_{GND}	Positive supply voltage to ground range	1.8		5.5	V
V_{REF}IN to A_{GND}	Reference input supply voltage to ground range	1.8		5.5	V
VIH, input high voltage	1.8 ≤ V_{DD} ≤ 2.7	V_{DD} - 0.3			V
VIH, input high voltage	2.7 < V_{DD} ≤ 5.5	2.4			V
VIL, input low voltage				0.5	V
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–65		150	°C

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7.4 Thermal Information

THERMAL METRIC(1)		DACx3608 RTE (WQFN) 16 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

All minimum/maximum specifications at T_A = -40°C to +125°C, 1.8V ≤ V_{DD} ≤ 5.5V, V_{REF}IN = 2.5V for V_{DD} ≥ 2.7 V, V_{REF}IN = 1.8V for V_{DD} ≤ 2.7 V, R_L=5kΩ to A_{GND}, C_L = 200pF to A_{GND}, Digital inputs at V_{DD} or A_{GND} unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
	Resolution	DAC53608	10			Bits
	Resolution	DAC43608	8			Bits
INL	Relative Accuracy(1)	DAC43608, 2.7V ≤ V_{DD} ≤ 5.5V	–1		1	LSB
INL	Relative Accuracy(1)	DAC43608, 1.8V ≤ V_{DD} ≤ 2.7V	–1		1	LSB
INL	Relative Accuracy(1)	DAC53608, 2.7V ≤ V_{DD} ≤ 5.5V	–1		1	LSB
INL	Relative Accuracy(1)	DAC53608, 1.8V ≤ V_{DD} ≤ 2.7V	–1		1	LSB
DNL	Differential Nonlinearity(1)	DAC43608, 2.7V ≤ V_{DD} ≤ 5.5V	–1		1	LSB
DNL	Differential Nonlinearity(1)	DAC43608, 1.8V ≤ V_{DD} ≤ 2.7V	–1		1	LSB
DNL	Differential Nonlinearity(1)	DAC53608, 2.7V ≤ V_{DD} ≤ 5.5V	–1		1	LSB
DNL	Differential Nonlinearity(1)	DAC53608, 1.8V ≤ V_{DD} ≤ 2.7V	–1		1	LSB
ZCE	Zero Code Error	2.7V ≤ V_{DD} ≤ 5.5V, Code 0d into DAC		6	12	mV
ZCE	Zero Code Error	1.8V ≤ V_{DD} ≤ 2.7V, Code 0d into DAC		6	12	mV
ZCE-TC	Zero Code Error Temperature Coefficient			±5		µV/°C
OE	Offset Error(1)	2.7V ≤ V_{DD} ≤ 5.5V	–0.5	0.25	0.5	%FSR
OE	Offset Error(1)	1.8V ≤ V_{DD} ≤ 2.7V	–1	0.5	1	%FSR
OE-TC	Offset Error Temperature Coefficient(1)			±0.0003		%FSR/°C
GE	Gain Error(1)	2.7V ≤ V_{DD} ≤ 5.5V	–0.5	0.25	0.5	%FSR
GE	Gain Error(1)	1.8V ≤ V_{DD} ≤ 2.7V	–1	0.5	1	%FSR
GE-TC	Gain Error Temperature Coefficient(1)			±0.0004		%FSR/°C
FSE	Full Scale Error	2.7V ≤ V_{DD} ≤ 5.5V, Code 1023d into DAC, No headroom	–0.5	0.25	0.5	%FSR
FSE	Full Scale Error	1.8V ≤ V_{DD} ≤ 2.7V, Code 1023d into DAC, No headroom	–1	0.5	1	%FSR
FSE-TC	Full Scale Error Temperature Coefficient			±0.0004		%FSR/°C
OUTPUT CHARACTERISTICS						
VOUT	Voltage Range		0		5.5	V
CLOAD	Max Capacitive Load	R_L = Infinite			1	nF
CLOAD	Max Capacitive Load	R_L = 5kΩ			2	nF
	Load regulation	DAC at midscale, -10mA ≤ I_{OUT} ≤ 10mA, V_{DD} = 5.5V		1.5		mV/mA
	Short circuit current	(per channel) full-scale output shorted to A_{GND}		50		mA
	Short circuit current	(per channel) zero output shorted to V_{DD}		50		mA
	Output Voltage Headroom	to V_{DD} (DAC output unloaded)		0.05		V
	Output Voltage Headroom	to V_{DD} (ILOAD = 10mA@V_{DD} = 5.5V, ILOAD = 3mA@V_{DD} = 2.7V, ILOAD = 1mA@V_{DD} = 1.8V), DAC code = Full Scale	10			%FSR
ZO	DC Output Impedance	DAC at midscale		0.25		Ω
ZO	DC Output Impedance	DAC at code 4d		0.25		Ω
ZO	DC Output Impedance	DAC at code 1016		0.26		Ω
DC-PSRR	Power Supply Rejection Ratio (DC)	DAC at midscale; V_{DD} = 5 V ± 10%		0.25		mV/V
DYNAMIC PERFORMANCE						

(1) End point fit between codes Code 4 to Code 1016 - 10 bit, Code 1 to Code 251 - 8 bit

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Electrical Characteristics (continued)

All minimum/maximum specifications at T_A = -40°C to +125°C, 1.8V ≤ V_{DD} ≤ 5.5V, V_{REF}IN = 2.5V for V_{DD} ≥ 2.7 V, V_{REF}IN = 1.8V for V_{DD} ≤ 2.7 V, R_L=5kΩ to A_{GND}, C_L = 200pF to A_{GND}, Digital inputs at V_{DD} or A_{GND} unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Tsett	Output Voltage Settling Time	1/4 to 3/4 scale and 3/4 to 1/4 scale settling to 10%FSR, R_L = 5K, C_L = 200pF, V_{DD} = 5.5V		10		µs
SR	Slew Rate	R_L = 5K, C_L = 200pF, V_{DD} = 5.5V		0.6		V/µs
	Power on Glitch Magnitude	R_L = 5K, C_L = 200pF		110		mV
Vnoisepp	Output Noise	0.1Hz to 10Hz, DAC at midscale, V_{DD} = 5.5V		40		uVpp
Vnoisepp	Output Noise	0.1Hz to 100kHz Bandwidth, DAC at midscale, V_{DD} = 5.5V		0.05		mVrms
Vnoise	Output Noise Density	measured at 1KHz, DAC at midscale, V_{DD} = 5.5V		0.2		µV/sqrtHz
Vnoise	Output Noise Density	measured at 10KHz, DAC at midscale, V_{DD} = 5.5V		0.2		µV/sqrtHz
AC-PSRR	Power Supply Rejection Ration (AC)	200mV 50/60Hz Sine wave superimposed on power supply voltage, DAC at midscale		-71		dB
	Channel-to-channel AC crosstalk	Full-scale swing on adjacent channel		10		nv-s
	Channel-to-channel DC crosstalk	Full-scale swing on all channel, Measured channel at zero or full scale		1		LSB
	Channel-to-channel digital crosstalk	DAC code mid scale, Adjacent input buffer change from ZS to FS or vice versa		10		nv-s
VGL	Code change glitch impulse	±1LSB change around mid code (including feedthrough)		4		nV-s
	Code change glitch impulse magnitude	±1LSB change around mid code (including feedthrough)		11		mV
VOLTAGE REFERENCE INPUT						
	Reference input impedance	All channel powered on		12.5		kΩ
	Reference input capacitance			50		pF
DIGITAL INPUTS						
	Digital feedthrough	At SCLK = 1MHz, DAC output static at mid scale		20		nV-s
	Pin Capacitance	Per pin		10		pF
POWER REQUIREMENTS						
IV_{DD}	Current Flowing into V_{DD}	Normal mode, All DACs at full scale. SPI static.		3	5	mA
IV_{DD}	Current Flowing into V_{DD}	All DACs power-down		50		µA

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7.6 Timing Requirements-I2C-Standard-Mode

All input signals are specified with $t_R = t_F$ = 1 ns/V (VIL to 70% of V_{DD}) and timed from a voltage level of (VIL + VIH) / 2. V_{DD} = 1.8 V to 5.5 V, V_{REF}IN = 1.8 V to 5.5 V, T_A = –40°C to +125°C, Vpull-up = V_{DD}; for V_{DD} 1.8V to 2.7V
Vpull-up = 2.7 or V_{DD}; for V_{DD} 2.7V to 5.5V

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			0.1	MHz
t_{BUF}	Bus free time between stop and start conditions	4.7			µs
t_{HDSTA}	Hold time after repeated start	4			µs
t_{SUSTA}	Repeated start setup time	4.7			µs
t_{SUSTO}	Stop condition setup time	4			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	250			ns
t_{LOW}	SCL clock low period	4700			ns
t_{HIGH}	SCL clock high period	4700			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			1000	ns

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7.7 Timing Requirements-I2C-Fast-Mode

All input signals are specified with $t_R = t_F$ = 1 ns/V (VIL to 70% of V_{DD}) and timed from a voltage level of (VIL + VIH) / 2. V_{DD} = 1.8 V to 5.5 V, V_{REF}IN = 1.8 V to 5.5 V, T_A = –40°C to +125°C, Vpull-up = V_{DD}; for V_{DD} 1.8V to 2.7V Vpull-up = 2.7 or V_{DD}; for V_{DD} 2.7V to 5.5V

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			0.4	MHz
t_{BUF}	Bus free time between stop and start conditions	1.3			µs
t_{HDSTA}	Hold time after repeated start	0.6			µs
t_{SUSTA}	Repeated start setup time	0.6			µs
t_{SUSTO}	Stop condition setup time	0.6			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_F	Clock and data fall time			300	ns
t_R	Clock and data rise time			300	ns

7.8 Timing Requirements-I2C-Fast-Plus-Mode

All input signals are specified with $t_R = t_F$ = 1 ns/V (VIL to 70% of V_{DD}) and timed from a voltage level of (VIL + VIH) / 2. V_{DD} = 1.8 V to 5.5 V, V_{REF}IN = 1.8 V to 5.5 V, T_A = – 40°C to + 125°C, Vpull up = V_{DD}; for V_{DD} 1.8 V to 2.7 V Vpull up = 2.7 or V_{DD}; for V_{DD} 2.7 V to 5.5 V

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCL frequency			1	MHz
t_{BUF}	Bus free time between stop and start conditions	0.5			µs
t_{HDSTA}	Hold time after repeated start	0.26			µs
t_{SUSTA}	Repeated start setup time	0.26			µs
t_{SUSTO}	Stop condition setup time	0.26			µs
t_{HDDAT}	Data hold time	0			ns
t_{SUDAT}	Data setup time	50			ns
t_{LOW}	SCL clock low period	0.5			µs
t_{HIGH}	SCL clock high period	0.26			µs
t_F	Clock and data fall time			120	ns
t_R	Clock and data rise time			120	ns

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7.9 Timing Requirements--Logic

All input signals are specified with $t_R = t_F$ = 1 ns/V (VIL to 70% of V_{DD}) and timed from a voltage level of (VIL + VIH) / 2. V_{DD} = 1.8 V to 5.5 V, V_{REF}IN = 1.8 V to 5.5 V, T_A = –40°C to +125°C, Vpull-up = V_{DD}; for V_{DD} 1.8V to 2.7V
Vpull-up = 2.7 or V_{DD}; for V_{DD} 2.7V to 5.5V

		MIN	NOM	MAX	UNIT
t_{LDACAH}	SCL Fall Edge to $\overline{LDAC}$ rise edge, 1.7 V ≤ V_{DD} ≤ 2.7 V	20			ns
t_{LDACAH}	SCL Fall Edge to $\overline{LDAC}$ rise edge, 2.7 V < V_{DD} ≤ 5.5 V	20			ns
t_{LDACAL}	$\overline{LDAC}$ fall edge to SCL fall edge, 1.7 V ≤ V_{DD} ≤ 2.7 V	20			ns
t_{LDACAL}	$\overline{LDAC}$ fall edge to SCL fall edge, 2.7 V < V_{DD} ≤ 5.5 V	20			ns
t_{LDACSH}	SCL Fall Edge to $\overline{LDAC}$ rise edge, 1.7 V ≤ V_{DD} ≤ 2.7 V	20			ns
t_{LDACSH}	SCL Fall Edge to $\overline{LDAC}$ rise edge, 2.7 V < V_{DD} ≤ 5.5 V	20			ns
t_{LDACSL}	SCL Fall Edge to $\overline{LDAC}$ fall edge, 1.7 V ≤ V_{DD} ≤ 2.7 V	20			ns
t_{LDACSL}	SCL Fall Edge to $\overline{LDAC}$ fall edge, 2.7 V < V_{DD} ≤ 5.5 V	20			ns
t_{LDACW}	$\overline{LDAC}$ low time, 1.7 V ≤ V_{DD} < 2.7 V	30			ns
t_{LDACW}	$\overline{LDAC}$ low time, 2.7 V ≤ V_{DD} ≤ 5.5 V	60			ns
t_{CLRW}	$\overline{CLR}$ low time, 1.7 V ≤ V_{DD} < 2.7 V	30			ns
t_{CLRW}	$\overline{CLR}$ low time, 2.7 V ≤ V_{DD} ≤ 5.5 V	60			ns
t_{SDU}	Successive DAC Updates, 1.7 V ≤ V_{DD} < 2.7 V	500			ns
t_{SDU}	Successive DAC Updates, 2.7 V ≤ V_{DD} ≤ 5.5 V	1000			ns

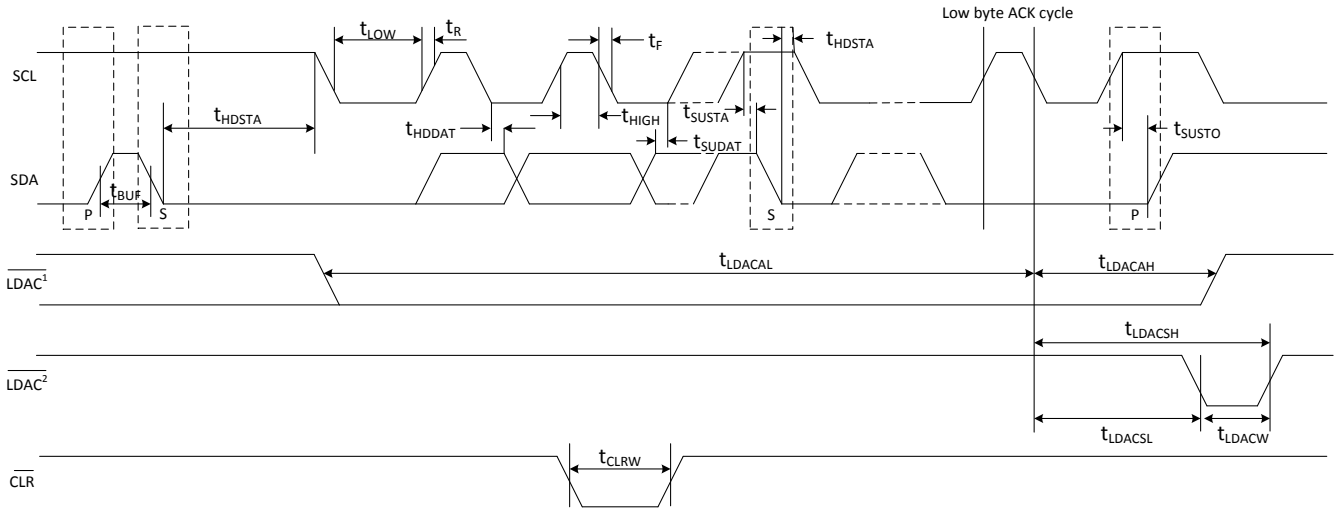

Figure 1. Timing

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8 Detailed Description

8.1 Overview

The DAC53608 and DAC43608 are a pin-compatible family of eight-channel, buffered voltage-output digital-to-analog converters (DACs) in 10- and 8-bit resolution. With an external reference ranging from 1.8 V to 5.5 V, full scale output voltage of 1.8 V to 5.5 V can be achieved. These devices are guaranteed monotonic across the power supply range.

Communication to the devices is done through I^{2}C^{TM} compatible interface. The I^{2}C^{TM} standard (100 kbps), fast (400 kbps), and fast+ mode (1Mbps) are supported for these devices. These devices include a load DAC (LDAC) pin for simultaneous DAC update.

The DAC53608 and DAC43608 incorporate a power-on-reset circuit that ensures the DAC outputs power up and remain at zero scale until a valid code is written to the device.

The DACx3608 devices are characterized for operation over the temperature range of -40°C to +125°C and are available in tiny QFN packages.

8.2 Functional Block Diagram

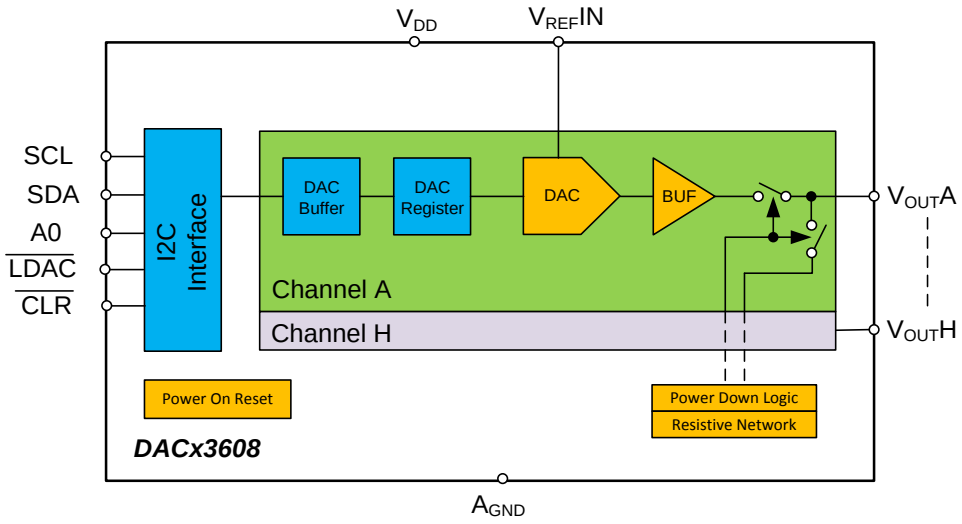

Figure 2. DACx3608 DAC Block Diagram

ADVANCE INFORMATION

8.3 Feature Description

8.3.1 Digital-to-Analog Converters (DACs) Architecture

Each output channel in the DACx3608 family of devices consists of string architecture with an output buffer amplifier. Figure 3 shows a block diagram of the DAC architecture.

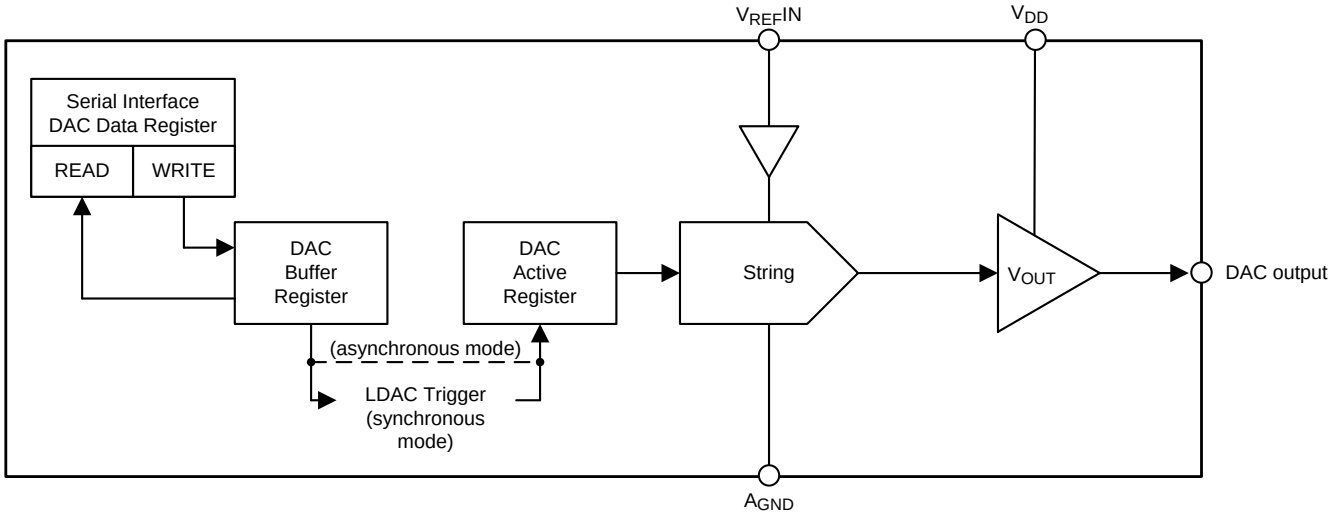

Figure 3. DACx3608 DAC Architecture

8.3.1.1 DAC Transfer Function

The device writes the input data to the individual DAC Data registers in straight binary format. After a power-on or a reset event, the device sets all DAC registers to zero-code. Equation 1 shows DAC transfer function.

$$V_{OUT}X = \frac{SDA}{2^n} \times V_{REF}IN \quad (1)$$

where:

- n is the resolution in bits (either 8 [DAC43608] or 10 [DAC53608])
- SDA is the decimal equivalent of the binary code that is loaded to the DAC register
- SDA ranges from 0 to $2^n - 1$
- $V_{REF}IN$ is the DAC reference voltage

8.3.1.2 DAC Register Update and $\overline{LDAC}$ Functionality

The device stores the data written to the DAC Data registers in the DAC buffer registers. Transfer of data from the DAC buffer registers to the active DAC registers can be set to happen immediately (asynchronous mode) or initiated by an $\overline{LDAC}$ trigger (synchronous mode). Once the DAC active registers are updated, the DAC outputs change to their new values. When the host reads from a DAC Data register, the value held in the DAC buffer register is returned (not the value held in the DAC active register).

The update mode for each DAC channel is determined by the status of $\overline{LDAC}$ pin.

In asynchronous mode ($\overline{LDAC}$ = 0 before the DAC write command), a write to the DAC data register results in an immediate update of the DAC active register and DAC output at the end of I^2C^{TM} frame.

In synchronous mode ($\overline{LDAC}$ = 1 before the DAC write command), writing to the DAC data register does not automatically update the DAC output. Instead the update occurs only after an $\overline{LDAC}$ is pulled to 0. The synchronous update mode enables simultaneous update of all DAC outputs.

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Feature Description (continued)

8.3.1.3 $\overline{CLR}$ Functionality

The $\overline{CLR}$ pin is an asynchronous input pin to the DAC. When this pin is pulled low (logic 0), the DAC buffers and the DAC latches to zero code.

8.3.1.4 Output Amplifier

The output buffer amplifier can generate rail-to-rail voltages on the output. The result is a maximum output range of 0 V to V_{DD}. The full-scale output range for each channel is determined by the reference voltage (V_{REF}IN) (Equation 1).

The buffer amplifier is capable of driving a load of TBD kΩ in parallel with TBD nF to GND. The typical slew rate is TBD V/µs with a typical ¼ to ¾ settling time of TBD µs.

8.3.2 Reference

The DACx3608 requires an external reference to operate. However, the reference pin V_{REF}IN and the supply pin V_{DD} can be tied together. The reference input pin voltage can range from 1.8 V to V_{DD}. The typical input impedance of this pin is when all the channels are powered on is 12.5 kΩ. The DACx3608 also includes LOW_VREF bit in the DEVICE_CONFIG register. For improved static performance when V_{REF}IN < 2.5 V, this bit must be set to 1.

8.3.3 Power-on-Reset (POR)

The DACx3608 family of devices includes a power-on reset function that controls the output voltage at power up. After the V_{DD} supply has been established a POR event is issued. The POR causes all registers to initialize to their default values and communication with the device is valid only after a 2-ms power-on-reset delay. The default value for all DACs in the DACx3608 devices is zero-code. At power-up all output channel buffer amplifiers start in power down to 10K mode until a power up command is issue by writing 0 to the per channel power down registers.

A power failure on V_{DD} also results in a power-on-reset event. As long as V_{DD} remains above their specified high threshold a power failure event will not occur. In order to ensure a V_{DD} collapse is registered as such by the device, these supplies must be below their corresponding low threshold for at least 1 ms. When the supplies drop below their high threshold but remain over the lower one (shown as the undefined region Figure 4), the device may or may not reset under all specified temperature and power-supply conditions.

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Feature Description (continued)

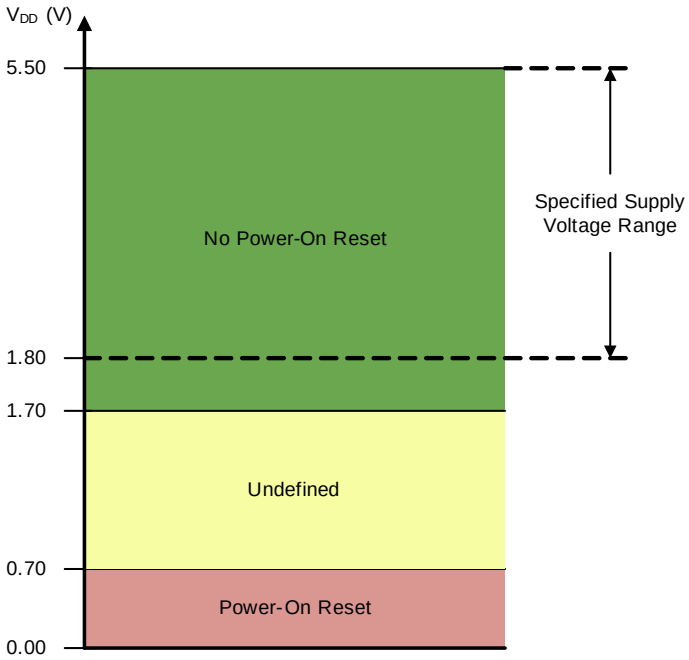

Figure 4. Threshold Levels for V_{DD} POR Circuit

8.3.4 Software Reset

When the device writes the reserved code 0x1010 to SW_RST in the TRIGGER register (address 0x02), the device initiates a software reset event.

8.4 Device Functional Modes

8.4.1 Power Down Mode

The DACx3608 DAC output amplifiers can be independently powered down (10K to A_{GND}) through the DEVICE_CONFIG register. In this state, the device consumes TBD µA (V_{DD} = 1.8 V). At power-up all output channels buffer amplifiers start in power down to 10K mode until a power up command is issue by writing 0 to the per channel power down registers.

8.5 Programming

The DACx3608 devices have a 2-wire serial interface: SCL, SDA, and one address pin, A0, as shown in Pin Configurations and Functions. The I^2C^{TM} bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C^{TM} compatible devices connects to the I^2C^{TM} bus through open drain I/O pins, SDA and SCL.

The I^2C^{TM} specification states that the device that controls communication is called a master, and the devices that are controlled by the master are called slaves. The master device generates the SCL signal. The master device also generates special timing conditions (start condition, repeated start condition, and stop condition) on the bus to indicate the start or stop of a data transfer. Device addressing is completed by the master. The master device on an I^2C^{TM} bus is typically a microcontroller or a digital signal processor (DSP). The DACx3608 family operates as a slave device on the I^2C^{TM} bus. A slave device acknowledges master's commands and upon master's control, receives or transmits data.

Typically, the DACx3608 family operates as a slave receiver. A master device writes to the DACx3608, a slave receiver. However, if a master device requires the DACx3608 internal register data, the DACx3608 family operates as a slave transmitter. In this case, the master device reads from the DACx3608 According to I^2C^{TM} terminology, read and write refer to the master device.

Programming (continued)

The DACx3608 family is a slave and supports the following data transfer modes:

- Standard mode (100 kbps)
- Fast mode (400 kbps)
- Fast mode+ (1.0 Mbps)

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. The fast mode+ protocol is supported in terms of data transfer speed, but not output current. The low-level output current would be 3 mA similar to the case of standard and fast modes. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as HS-mode. The DACx3608 family supports 7-bit addressing. The 10-bit addressing mode is not supported. The device supports the general call reset function. Sending the following sequence initiates a software reset within the device; Start/Repeated Start, 0x00, 0x06, Stop. The reset is asserted within the device on the falling edge of the ACK bit, following the second byte.

Other than specific timing signals, the I^{2}C^{TM} interface works with serial bytes. At the end of each byte, a ninth clock cycle generates and detects an acknowledge signal. Acknowledge is when the SDA line is pulled low during the high period of the ninth clock cycle. A not-acknowledge is when the SDA line is left high during the high period of the ninth clock cycle as shown in Figure 5.

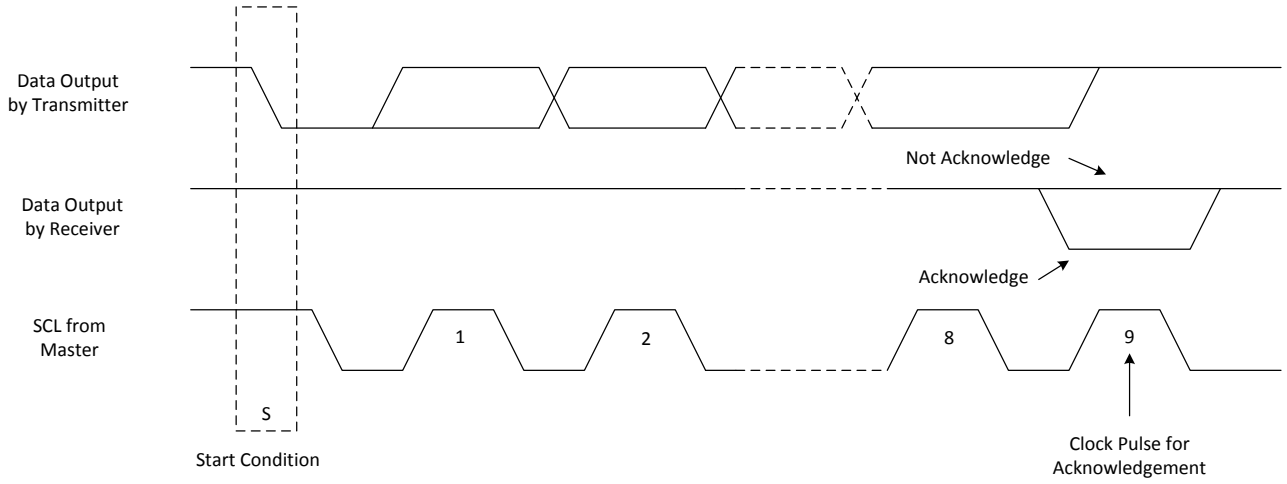

Figure 5. Acknowledge and Not Acknowledge on the I^{2}C Bus

8.5.1 F/S Mode Protocol

1. The master initiates data transfer by generating a start condition. The start condition is when a high to-low transition occurs on the SDA line while SCL is high, as shown in Figure 6. All I^{2}C^{TM} compatible devices recognize a start condition.

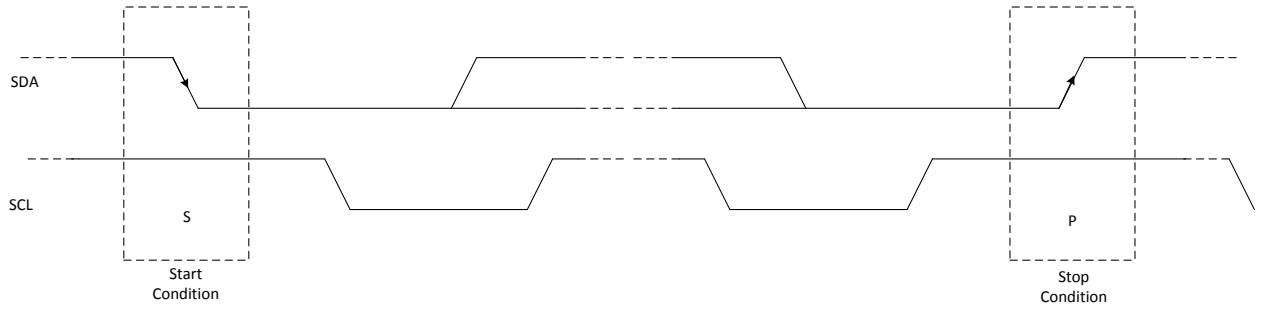

Figure 6. Start and Stop Conditions

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Programming (continued)

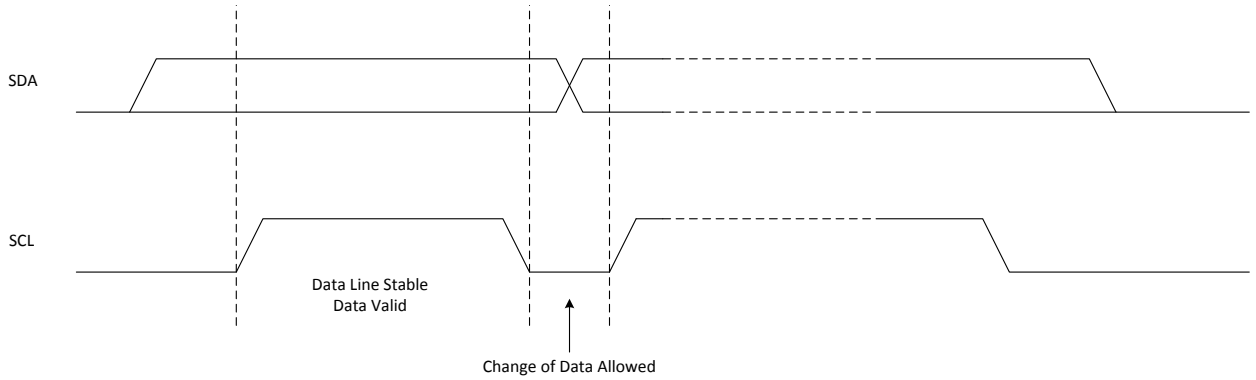

Figure 7. Bit Transfer on the I²C Bus

2. The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/W) on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in Figure 7. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the 9th SCL cycle, as shown in Figure 5 by pulling the SDA line low during the entire high period of the 9th SCL cycle. Upon detecting this acknowledge, the master knows the communication link with a slave has been established.
3. The master generates further SCL cycles to transmit (R/W bit 0) or receive (R/W bit 1) data to the slave. In either case, the receiver must acknowledge the data sent by the transmitter. So the acknowledge signal can be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consists of 8-data bits and 1 acknowledge-bit, and can continue as long as necessary.
4. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 6). This action releases the bus and stops the communication link with the addressed slave. All I²C™-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all slave devices then wait for a start condition followed by a matching address.

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Programming (continued)

8.5.2 DACx3608 I²C Update Sequence

For a single update, the DACx3608 requires a start condition, a valid I²C™ address byte, a command byte, and two data bytes (the most significant data byte (MSDB) and least significant data byte (LSDB)), as listed in Table 1.

Table 1. Update Sequence

MSB	....	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK	MSB	...	LSB	ACK
Address (A) byte				Command byte				MSDB				LSDB			
DB [32:24]				DB [23:16]				DB [15:8]				DB [7:0]			

After each byte is received, the DACx3608 family acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse, as shown in Figure 8. These four bytes and acknowledge cycles make up the 36 clock cycles required for a single update to occur. A valid I²C™ address byte selects the DACx3608 devices.

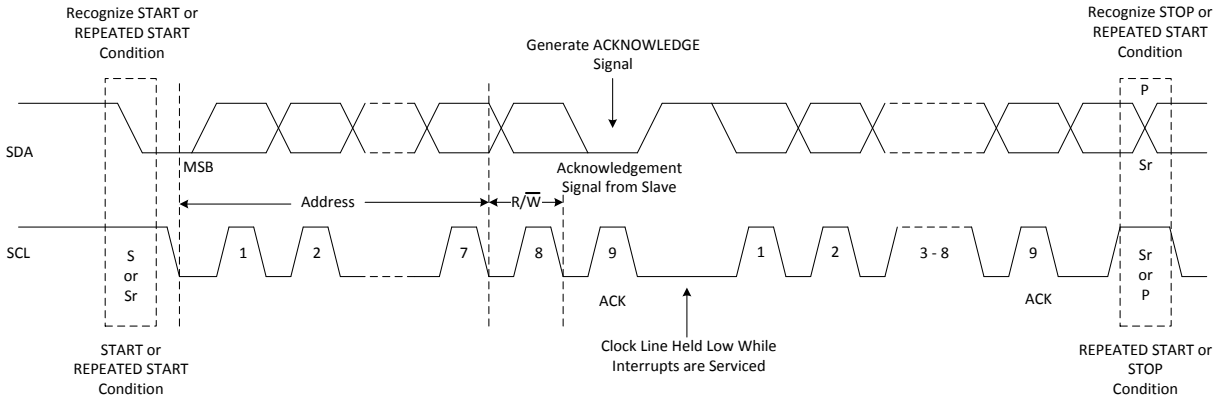

Figure 8. I²C Bus Protocol

The command byte sets the operational mode of the selected DACx3608 device. When the operational mode is selected by this byte, the DACx3608 series must receive two data bytes, the most significant data byte (MSDB) and least significant data byte (LSDB), for a data update to occur. The DACx3608 devices perform an update on the falling edge of the acknowledge signal that follows the LSDB.

When using fast mode (clock = 400 kHz), the maximum DAC update rate is limited to 22.22 kSPS. Using the fast mode+ (clock = 1 MHz), the maximum DAC update rate is limited to 55.55 kSPS. When a stop condition is received, the DACx3608 family releases the I²C™ bus and awaits a new start condition.

8.5.3 DACx3608 Address Byte

The address byte, as shown in Table 2, is the first byte received following the START condition from the master device. The first four bits (MSBs) of the address are factory preset to 1001. The next 3 bits of the address are controlled by the A0 pin. The A0 pin input can be connected to V_{DD}, A_{GND}, SCL, or SDA. The A0 pin is sampled during the first byte of each data frame to determine the address. The device latches the value of the address pin and consequently will respond to that particular address according to Table 3.

The DACx3608 family supports broadcast addressing. Broadcast addressing can be used for synchronously updating or powering down multiple DACx3608 devices. The DACx3608 family is designed to work with other members of the family to support multichip synchronous update. Using the broadcast address, the DACx3608 devices respond regardless of the states of the address pins. Broadcast is supported only in write mode.

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Table 2. DACx3608 Address Byte

COMMENT	MSB							LSB
	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/$\overline{W}$
General address	1	0	0	1	See Table 3 (slave address column)			0 or 1
Broadcast address	1	0	0	0	1	1	1	0

Table 3. Address Format

SLAVE ADDRESS	A0 PIN
1001 000	0
1001 001	1
1001 010	SDA
1001 011	SCL

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8.5.4 DACx3608 Command Byte

The DACx3608 command byte (shown in Table 4) controls which command is executed and which register is being accessed when writing to or reading from the DACx3608 series.

Table 4. DACx3608 Command Byte

B23	B22	B21	B20	B19	B18	B17	B16	COMMENT
0	0	0	0	0	0	0	0	No Operation
0	0	0	0	0	0	0	1	DEVICE_CONFIG
0	0	0	0	0	0	1	0	STATUS/TRIGGER
0	0	0	0	0	0	1	1	BRDCAST
0	0	0	0	1	0	0	0	DACA_DATA
0	0	0	0	1	0	0	1	DACB_DATA
0	0	0	0	1	0	1	0	DACC_DATA
0	0	0	0	1	0	1	1	DACD_DATA
0	0	0	0	1	1	0	0	DACE_DATA
0	0	0	0	1	1	0	1	DACF_DATA
0	0	0	0	1	1	1	0	DACG_DATA
0	0	0	0	1	1	1	1	DACH_DATA

8.5.5 DACx3608 Data Byte (MSDB and LSDB)

The MSDB and LSDB contain the data that are passed to the register(s) specified by the command byte as shown in Table 5. The DACx3608 family updates at the falling edge of the acknowledge signal that follows the LSDB[0] bit.

Table 5. DACx3608 Data Byte

COMMAND BITS	DATA BITS												
	MSDB				LSDB								
B19 - B16	B15 - B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
NOP	x	0	0	0	0	0	0	0	0	0	0	0	0
DEVICE_CONFIG	x	0	0	LOW_VREF	PDN-All	PDNH	PDNG	PDNF	PDNE	PDND	PDNC	PDNB	PDNA
STATUS/TRIGGER	x	DEVICE_ID						x	x	SW_RST			
BRDCAST	x	BRDCAST_DATA[9:0] / BRDCAST_DATA[7:0] – MSB left aligned										x	x
DACA_DATA	x	DACA_DATA[9:0] / DACA_DATA[7:0] – MSB left aligned										x	x
DACB_DATA	x	DACB_DATA[9:0] / DACB_DATA[7:0] – MSB left aligned										x	x
DACC_DATA	x	DACC_DATA[9:0] / DACC_DATA[7:0] – MSB left aligned										x	x
DACD_DATA	x	DACD_DATA[9:0] / DACD_DATA[7:0] – MSB left aligned										x	x
DACE_DATA	x	DACE_DATA[9:0] / DACE_DATA[7:0] – MSB left aligned										x	x
DACF_DATA	x	DACF_DATA[9:0] / DACF_DATA[7:0] – MSB left aligned										x	x
DACG_DATA	x	DACG_DATA[9:0] / DACG_DATA[7:0] – MSB left aligned										x	x
DACH_DATA	x	DACH_DATA[9:0] / DACAH_DATA[7:0] – MSB left aligned										x	x

8.5.6 DACx3608 I²C™ Read Sequence

To read any register the following command sequence must be used:

1. Send a start or repeated start command with a slave address and the R/$\overline{W}$ bit set to 0 for writing. The device acknowledges this event.
2. Send a command byte for the register to be read. The device acknowledges this event again.
3. Send a repeated start with the slave address and the R/$\overline{W}$ bit set to '1' for reading. The device acknowledges this event.
4. The device writes the MSDB byte of the addressed register. The master must acknowledge this byte. Finally,

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the device writes out the LSDB of the register.

An alternative reading method allows for reading back the value of the last register written. The sequence is a start or repeated start with the slave address and the R/$\overline{W}$ bit set to 1, and the two bytes of the last register are read out. All the registers in DACx3608 family can be read out with the exception of SW-RST register. Table 5 shows the read command set.

Note that it is not possible to use the broadcast address for reading.

Table 6. Read Sequence

S	MSB	…	R/$\overline{W}$ (0)	ACK	MSB	…	LSB	ACK	Sr	MSB	…	R/$\overline{W}$ (1)	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
	ADDRESS BYTE				COMMAND BYTE				Sr	ADDRESS BYTE				MSDB				LSDB			
From Master				Slave	From Master			Slave	From Master				Slave	From Slave			Master	From Slave			Master

8.6 Register Map

Table 7. Register Address

B23	B22	B21	B20	B19	B18	B17	B16	COMMENT
0	0	0	0	0	0	0	0	No Operation
0	0	0	0	0	0	0	1	DEVICE_CONFIG
0	0	0	0	0	0	1	0	STATUS/TRIGGER
0	0	0	0	0	0	1	1	BRDCAST
0	0	0	0	1	0	0	0	DACA_DATA
0	0	0	0	1	0	0	1	DACB_DATA
0	0	0	0	1	0	1	0	DACC_DATA
0	0	0	0	1	0	1	1	DACD_DATA
0	0	0	0	1	1	0	0	DACE_DATA
0	0	0	0	1	1	0	1	DACF_DATA
0	0	0	0	1	1	1	0	DACG_DATA
0	0	0	0	1	1	1	1	DACH_DATA

Table 8. Register Map

COMMAND BITS	DATA BITS												
	MSDB				LSDB								
B19 - B16	B15 - B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
NOP	x	0	0	0	0	0	0	0	0	0	0	0	0
DEVICE_CONFIG	x	0	0	LOW_VREF	x	PDNH	PDNG	PDNF	PDNE	PDND	PDNC	PDNB	PDNA
STATUS/TRIGGER	x	DEVICE_ID						x	x	SW_RST			
BRDCAST	x	BRDCAST_DATA[9:0] / BRDCAST_DATA[7:0] – MSB left aligned										x	x
DACA_DATA	x	DACA_DATA[9:0] / DACA_DATA[7:0] – MSB left aligned										x	x
DACB_DATA	x	DACB_DATA[9:0] / DACB_DATA[7:0] – MSB left aligned										x	x
DACC_DATA	x	DACC_DATA[9:0] / DACC_DATA[7:0] – MSB left aligned										x	x
DACD_DATA	x	DACD_DATA[9:0] / DACD_DATA[7:0] – MSB left aligned										x	x
DACE_DATA	x	DACE_DATA[9:0] / DACE_DATA[7:0] – MSB left aligned										x	x
DACF_DATA	x	DACF_DATA[9:0] / DACF_DATA[7:0] – MSB left aligned										x	x
DACG_DATA	x	DACG_DATA[9:0] / DACG_DATA[7:0] – MSB left aligned										x	x
DACH_DATA	x	DACH_DATA[9:0] / DACAH_DATA[7:0] – MSB left aligned										x	x

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Table 9. DACx3608 Register Names

OFFSET	ACRONYM	REGISTER NAME	SECTION
00h	NOP	No Operation	NOP Register (offset = 00h)
01h	DEVICE_CONFIG	Device Configuration Register	DEVICE_CONFIG Register (offset = 01h)
02h	STATUS/TRIGGER	Status and Trigger Register	STATUS/TRIGGER Register (offset = 02h)
03h	BRDCAST	Broadcast Data Register	BRDCAST Register (offset = 03h)
08h - 0Fh	DACA_DATA	DACn Data Register	DACn_DATA Register (offset = 08h - 0Fh)

8.6.1 NOP Register (offset = 00h)

Figure 9. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Don't Care															
$\overline{W}$															

Table 10. NOP Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-0	Don't Care	$\overline{W}$	0000h	Don't Care

8.6.2 DEVICE_CONFIG Register (offset = 01h)

Figure 10. DEVICE_CONFIG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Don't Care				0	0	LOW_VREF	PDN-AlII	PDNH	PDNG	PDNF	PDNE	PDND	PDNC	PDNB	PDNA
$\overline{W}$				R/$\overline{W}$				R/$\overline{W}$							

Table 11. DEVICE_CONFIG Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	Don't Care	$\overline{W}$	0h	Don't Care
11-10	RESERVED	$\overline{W}$	00	Reserved
9	LOW_VREF	R/$\overline{W}$	0	Set to '1' when V_{REF}IN < 2.5 V else set to '0'
8	PDN-All	R/$\overline{W}$	0	Global power down bit, When set to '1', all channels and all bias blocks are powered down
7-0	PDNn	R/$\overline{W}$	00h	DACn in power down mode (Output buffers power down 10K to A_{GND}) when this bit is set to '1'

8.6.3 STATUS/TRIGGER Register (offset = 02h)

Figure 11. STATUS/TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Don't Care				DEVICE_ID						Don't Care	Don't Care	SW_RST			
$\overline{W}$				R						$\overline{W}$	$\overline{W}$	$\overline{W}$			

Table 12. STATUS/TRIGGER Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	Don't Care	$\overline{W}$	0h	Don't Care
11-6	DEVICE_ID	R	000000	Device Identification number
5-4	Don't Care	$\overline{W}$	0h	Don't Care

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Table 12. STATUS/TRIGGER Register Field Descriptions (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
3-0	SW_RST	W	0h	Device resets to default value when this register is set to 1010

8.6.4 BRDCAST Register (offset = 03h)

Figure 12. BRDCAST Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Don't Care				BRDCAST_DATA[9:0] / BRDCAST_DATA[7:0] – MSB Left aligned										Don't Care	Don't Care
W				W										W	W

Table 13. BRDCAST Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	Don't Care	W	0h	Don't Care
11-2	BRDCAST_DATA[9:0] / BRDCAST_DATA[7:0]	W	000h	Writing to the BRDCAST register forces the DAC channel to update its active register data to the BRDCAST_DATA one. Data is LSB aligned in straight binary format and follows the format below: DAC53608: { DATA[9:0] } DAC43608: { DATA[7:0], x, x } x – Don't care bits
1-0	Don't Care	W	00	Don't Care

8.6.5 DACn_DATA Register (offset = 08h - 0Fh)

Figure 13. DACn_DATA Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Don't Care				BRDCAST_DATA[9:0] / BRDCAST_DATA[7:0] – MSB Left aligned										Don't Care	Don't Care
W				W										W	W

Table 14. DACn_DATA Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-12	Don't Care	W	0h	Don't Care
11-2	DACn_DATA[9:0] / DACn_DATA[7:0]	W	000h	Writing to the DACn_DATA register forces the respective DAC channel to update its active register data to the DACn_DATA. Data is LSB aligned in straight binary format and follows the format below: DAC53608: { DATA[9:0] } DAC43608: { DATA[7:0], x, x } x – Don't care bits
1-0	Don't Care	W	00	Don't Care

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DACx3608 is a buffered output, 8-channel, low power DAC available in a tiny 3X3 package. The multi-channel, low power, and small package makes this DAC suitable for general purpose applications in wide range of end equipments. Some of the most common applications for this devices are LED biasing in multi-function printers, power supply supervision with programmable comparators, offset and gain trimming in precision circuits, and power supply margining.

9.2 Typical Applications

9.2.1 Programmable LED Biasing

End equipments such as multi-function printers, projectors and electronic point-of-sale (EPOS) require a steady luminous intensity from the LED. Figure 14 shows a simplified circuit diagram for biasing an LED using DACx3608.

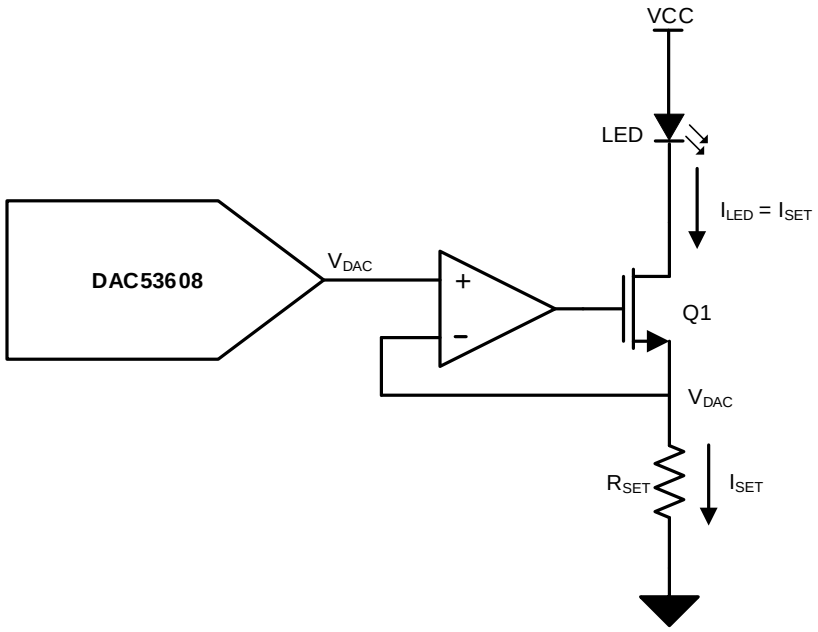

Figure 14. LED Biasing

9.2.1.1 Design Requirements

- Programmable Constant Current through an LED tied to power supply on one end
- DAC Output Range: 0 – 5 V
- LED Current Range: 0 – 20 mA

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Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

The DAC is used to set the source current of a MOSFET using a unity-gain buffer as shown in Figure 14. The LED is connected between the power supply and the drain of the MOSFET. This configuration allows the DAC to control or set the amount of current through the LED. The buffer following the DAC controls the gate-source voltage of the MOSFET inside the feedback loop thus compensating this drop and corresponding drift due to temperature, current, and ageing of the MOSFET. The current set by the DAC that flows through the LED can be calculated with Equation 2. in order to generate 0 – 20mA from a 0 – 5 V DAC output range, a 250-Ω $R_{SET}$is required.

$$I_{SET} = \frac{V_{DAC}}{R_{SET}} \tag{2}$$

The pseudocode for getting started with the LED biasing application is given below.

```
//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <DATA>
//Power-up the device and channels
WRITE DEVICE_CONFIG(0x01), 0x0000
//Program mid code (or the desired voltage) on all channels
WRITE DACA_DATA(0x08), 0x07FC //12-bit MSB aligned
WRITE DACB_DATA(0x09), 0x07FC //12-bit MSB aligned
WRITE DACC_DATA(0x0A), 0x07FC //12-bit MSB aligned
WRITE DACD_DATA(0x0B), 0x07FC //12-bit MSB aligned
WRITE DACE_DATA(0x0C), 0x07FC //12-bit MSB aligned
WRITE DACF_DATA(0x0D), 0x07FC //12-bit MSB aligned
WRITE DACG_DATA(0x0E), 0x07FC //12-bit MSB aligned
WRITE DACH_DATA(0x0F), 0x07FC //12-bit MSB aligned
```

9.2.2 Programmable Window Comparator

End equipments that use a centralized power supply such as network servers, optical modules, and others require the monitoring of power buses in order to protect the components. This monitoring or supervision is accomplished using a window comparator. A window comparator monitors a signal input for upper and lower threshold violations. A trigger signal is generated when the threshold violations occur. Multi-channel monitoring is required in order to supervise all power supplies available in a module. DACx3608 provides a easy to use, low-footprint method to address this requirement.

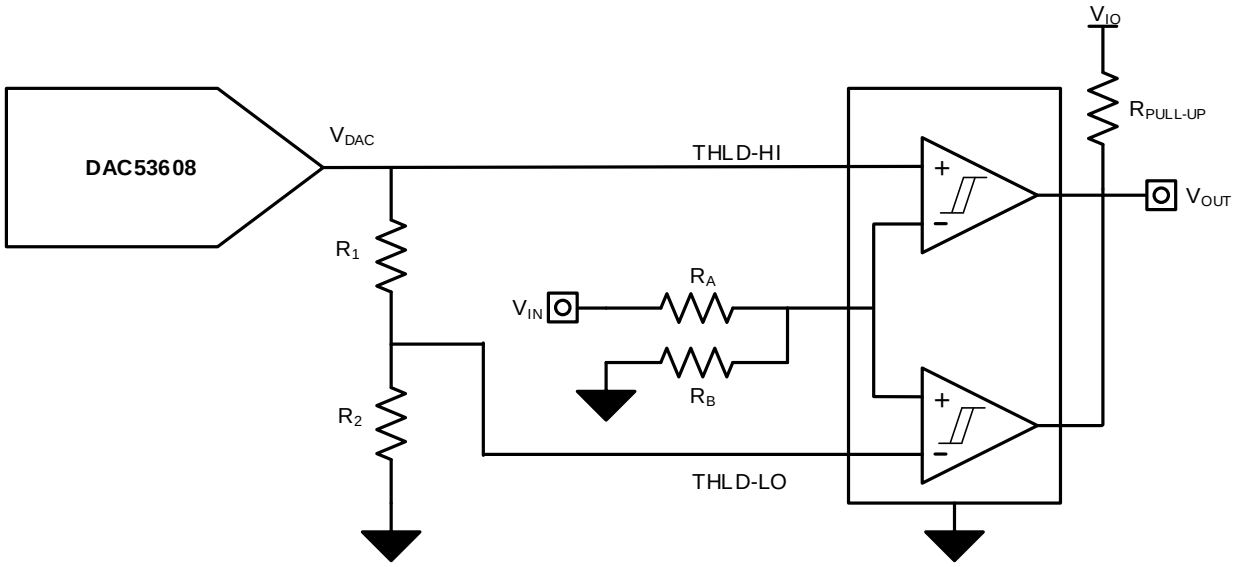

Figure 15. Programmable Window Comparator

Typical Applications (continued)

9.2.2.1 Design Requirements

- Voltage to be Monitored: 5 V
- High Threshold: 5 V + 10%
- Low Threshold: 5 V – 10%
- Trigger Output: 3.3-V Open-Drain Single Output

9.2.2.2 Detailed Design Procedure

Figure 15 provides an example in which single DAC channel is used to compare both high and low thresholds. A dual comparator is used per DAC channel as shown. A voltage divider formed by resistors R_A and R_B are used in order to bring the signal level within the DAC range. Another pair of resistors R_1 and R_2 are used for setting the low threshold as a factor of the high threshold. This configuration allows the use of a single DAC channel for monitoring both high and low threshold levels. The comparators should be open-drain in order to provide the following advantages.

- Generate a logic output level suitable for the monitoring processor
- Allow shorting of the two outputs in order to generate a single trigger

In the circuit depicted in Figure 15 the output of the circuit remains HIGH as long as the signal input remains within the high and low threshold levels. Upon violation of any one threshold, the output goes LOW. Equation 3 provides the derivation of the low threshold voltage from the high threshold set by the DAC.

$$V_{THLD\text{-}LO} = V_{DAC} \times \left(\frac{R_2}{R_1 + R_2} \right) \tag{3}$$

In order to monitor a power supply of 5 V within ±10%, it is recommended to place the nominal value at the DAC mid code. The output range of DACx3608 to be 0 – 5 V, thus the mid code voltage output is 2.5 V. Hence, R_A and R_B can be chosen in such a way that the voltage to be compared is 2.5 V. For this example, R_A is equal to R_B and we can use 10-kΩ resistors for both of them. One channel of the DACx3608 must be programmed to $V_{THLD\text{-}HI}$, for example 2.5 V + 5% = 2.625 V. This corresponds to a 10-bit DAC code of ($2^{10} \div 5$ V) × 2.625 V = 537.6 (0x21 Ah). In order to generate $V_{THLD\text{-}LO}$(for example, 2.5 V – 5% = 2.405 V) from 2.625 V, the values of R_1 and R_2 can be calculated as 7.5 kΩ and 82 kΩ, respectively using Equation 3. The pseudocode for getting started with the programmable window comparator application with the desired DAC value is given below.

```
//SYNTAX: WRITE <REGISTER NAME(Hex Code)>, <DATA>
//Power-up the device and channels
WRITE DEVICE_CONFIG(0x01), 0x0000
//Program 2.625V on channel A
WRITE DACA_DATA(0x08), 0x0868 //12-bit MSB aligned
```

ADVANCE INFORMATION

10 Power Supply Recommendations

The DACx3608 family of devices does not require specific supply sequencing. It requires a single power supply, VDD. A 0.1-µF decoupling capacitor is recommended for the VDD pin.

11 Layout

11.1 Layout Guidelines

The DACx3608 pinout separates the analog, digital, and power pins for an optimized layout. For signal integrity, it is recommended that digital and analog traces be separated and decoupling capacitors places close with the device pins.

11.2 Layout Example

Figure 16 shows an example layout drawing with decoupling capacitors and pull-up resistors.

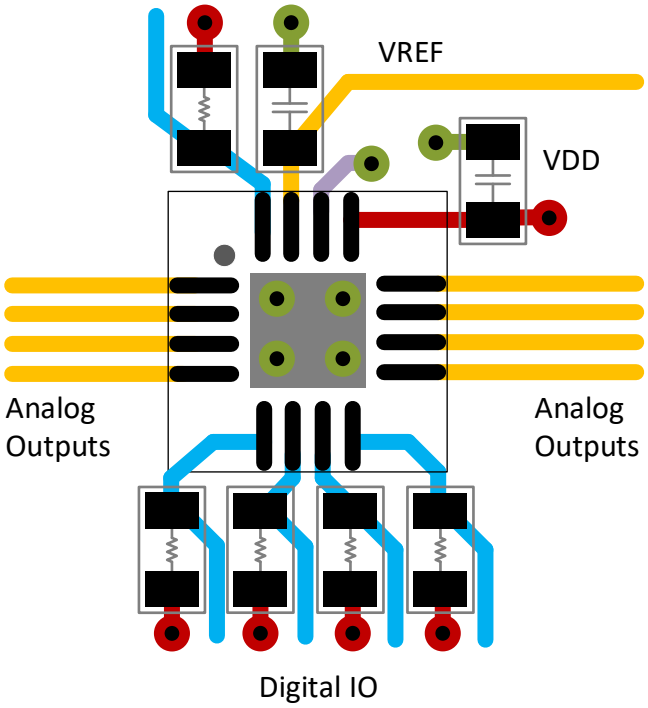

Figure 16. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following: *DAC53608EVM User's Guide* (SLAU790)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 15. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DAC53608	Click here	Click here	Click here	Click here	Click here
DAC43608	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC43608RTER	PREVIEW	WQFN	RTE	16	3000	TBD	Call TI	Call TI	-40 to 125		
DAC43608RTET	PREVIEW	WQFN	RTE	16	250	TBD	Call TI	Call TI	-40 to 125		
DAC53608RTER	PREVIEW	WQFN	RTE	16	250	TBD	Call TI	Call TI	-40 to 125		
DAC53608RTET	PREVIEW	WQFN	RTE	16	250	TBD	Call TI	Call TI	-40 to 125		
PDAC53608RTET	ACTIVE	WQFN	RTE	16	250	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

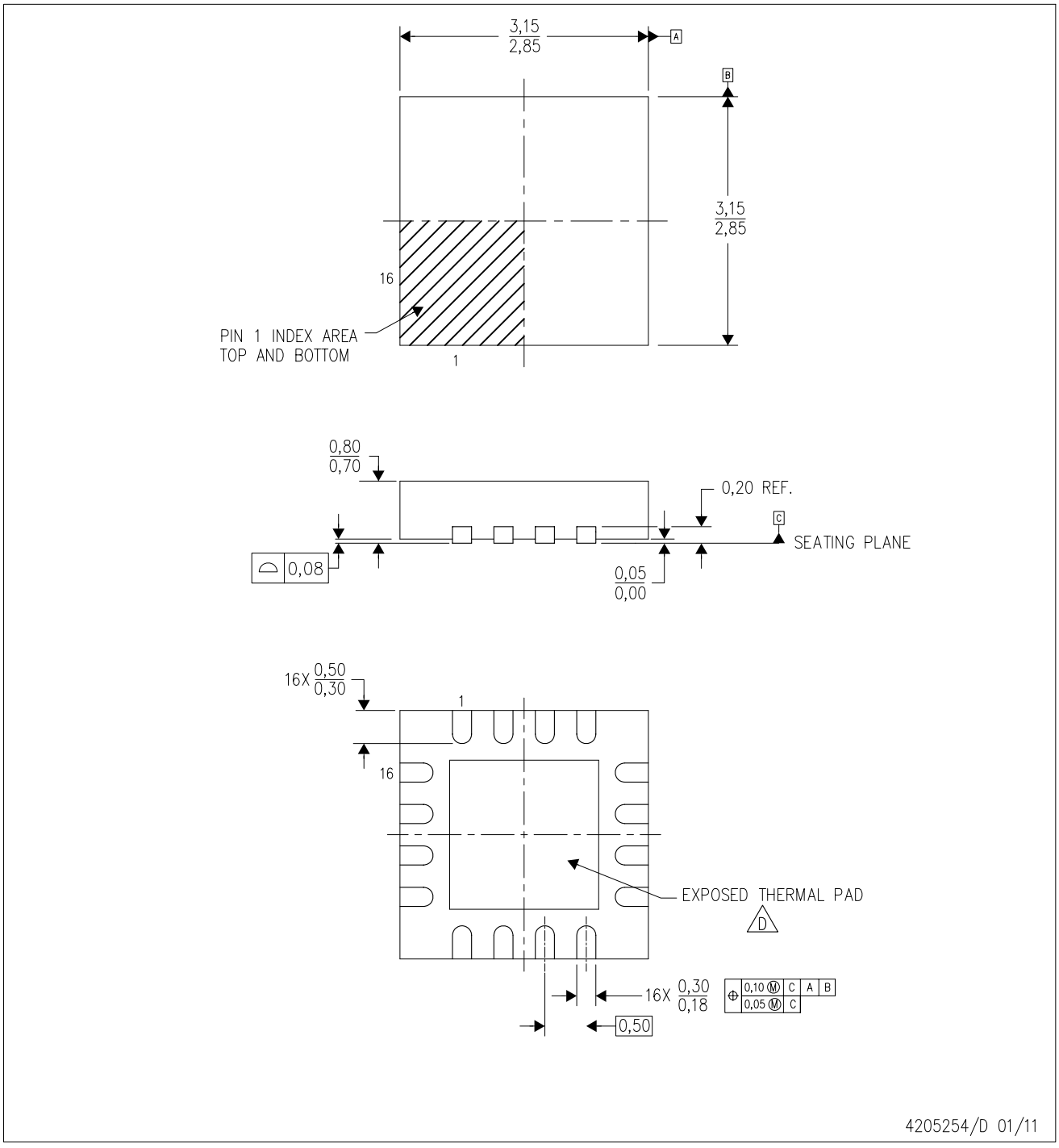
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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