

# **BUK9Y25-80E**

## N-channel 80 V, 27 mΩ logic level MOSFET in LFPAK56 Product data sheet

#### 1. **General description**

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

#### 2. **Features and benefits**

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V<sub>GS(th)</sub> rating of greater than 0.5 V at 175 °C

#### **Applications** 3.

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

### Quick reference data

Quick reference data Table 1.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	-	80	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	37	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	-	95	W
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$		-	22.2	27	mΩ
Dynamic characteristics							
$Q_{GD}$	gate-drain charge	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; V_{DS} = 64 \text{ V};$ $T_j = 25 \text{ °C}; \underline{\text{Fig. 13}}; \underline{\text{Fig. 14}}$		-	5.8	-	nC



#### N-channel 80 V, 27 m $\Omega$ logic level MOSFET in LFPAK56

# 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	q	G_U: 4
4	G	gate	و ق ق ق	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

# 6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK9Y25-80E	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669		

# 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y25-80E	92580E

# 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	80	V
$V_{DGR}$	drain-gate voltage	$R_{GS}$ = 20 k $\Omega$		-	80	V
$V_{GS}$	gate-source voltage	T <sub>j</sub> ≤ 175 °C; DC		-10	10	V
		T <sub>j</sub> ≤ 175 °C; Pulsed	[1][2]	-15	15	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 5 V; <u>Fig. 1</u>		-	37	Α
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 5 V; <u>Fig. 1</u>		-	26.5	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; pulsed; $t_p \le 10 \mu s$ ; Fig. 4		-	150	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	95	W

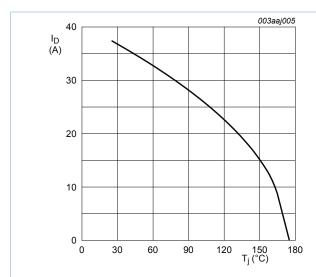
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### N-channel 80 V, 27 mΩ logic level MOSFET in LFPAK56

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
Source-drain	diode					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	37	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	150	Α
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 37 A; $V_{sup} \le 80$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3	[3][4]	-	45.4	mJ

- Accumulated pulse duration up to 50 hours delivers zero defect ppm Significantly longer life times are achieved by lowering  $\rm T_j$  and or  $\rm V_{GS}$
- [2]
- Single-pulse avalanche rating limited by maximum junction temperature of 175 °C. [3]
- Refer to application note AN10273 for further information.



Continuous drain current as a function of Fig. 1. mounting base temperature

 $V_{GS} \ge 5V$ 

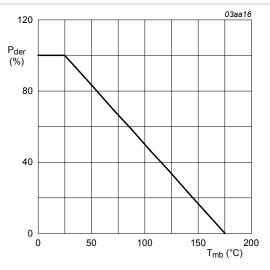


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

#### N-channel 80 V, 27 m $\Omega$ logic level MOSFET in LFPAK56

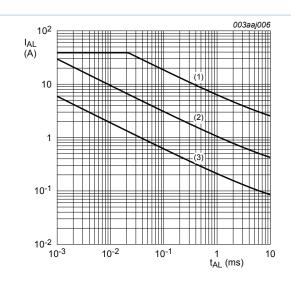
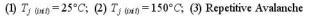


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time



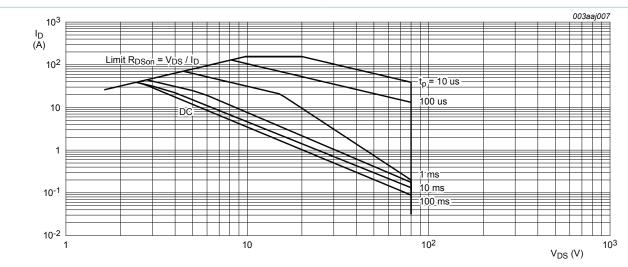


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

### 9. Thermal characteristics

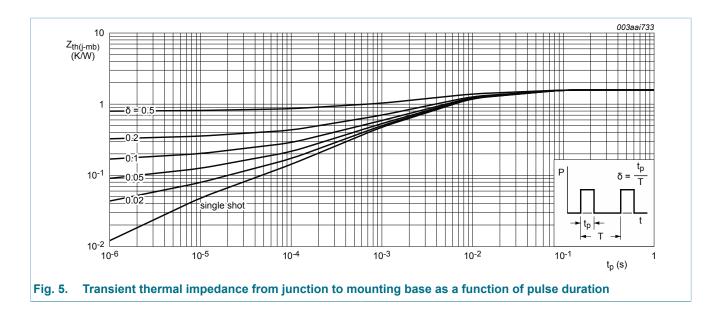
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	-	1.58	K/W

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#### N-channel 80 V, 27 m $\Omega$ logic level MOSFET in LFPAK56



## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V <sub>(BR)DSS</sub>	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	80	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = -55 °C; Fig. 9	-	-	2.45	V
	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	0.5	-	-	V	
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.1	1	μA
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 ^{\circ}\text{C}; Fig. 11$	-	22.2	27	mΩ
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; Fig. 11	-	20.5	25	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 175 °C; Fig. 12; Fig. 11	-	-	67.8	mΩ

### N-channel 80 V, 27 m $\Omega$ logic level MOSFET in LFPAK56

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Dynamic cl	naracteristics		'			
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 64 V; V <sub>GS</sub> = 5 V;	-	17.1	-	nC
Q <sub>GS</sub>	gate-source charge	T <sub>j</sub> = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	5.2	-	nC
$Q_{GD}$	gate-drain charge		-	5.8	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <u>Fig. 15</u>	-	2032	2703	pF
C <sub>oss</sub>	output capacitance		-	147	176	pF
C <sub>rss</sub>	reverse transfer capacitance		-	75	103	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 60 V; R <sub>L</sub> = 4.98 Ω; V <sub>GS</sub> = 5 V;	-	11.6	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 °C$	-	17.2	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	23.9	-	ns
t <sub>f</sub>	fall time		-	15.3	-	ns
Source-dra	in diode					
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 10 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <u>Fig. 16</u>	-	0.81	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 10 \text{ A}; \text{ d}I_S/\text{d}t = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$	-	23.8	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 25 V; T <sub>j</sub> = 25 °C	-	27	-	nC

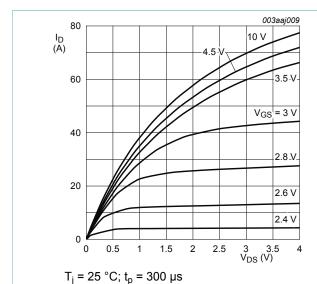


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

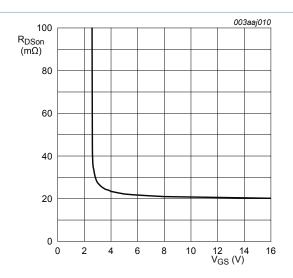


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25$$
°C;  $I_D = 10A$ 

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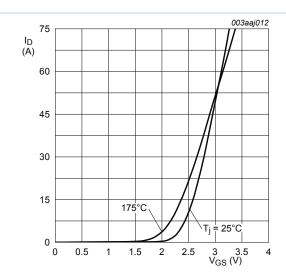


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



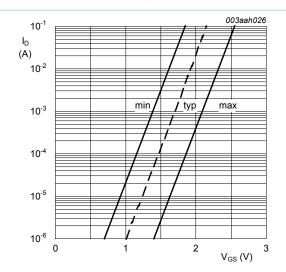


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25$$
°C;  $V_{DS} = 5V$ 

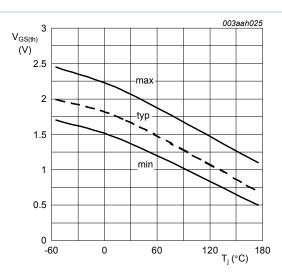
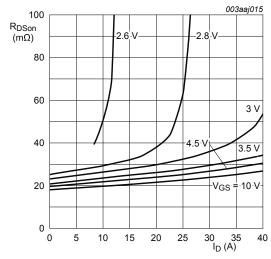


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1$$
 mA;  $V_{DS} = V_{GS}$ 



 $T_i = 25 \,^{\circ}\text{C}; t_p = 300 \,\mu\text{s}$ 

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

### N-channel 80 V, 27 mΩ logic level MOSFET in LFPAK56

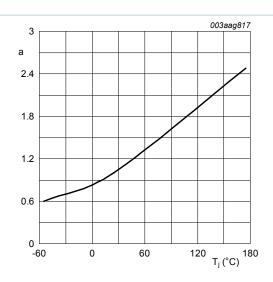


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\mathbf{a} = \frac{R_{DSon}}{R_{DSon(25\ \mathrm{C})}}$$

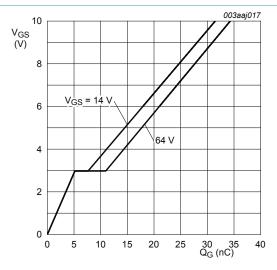


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 10A$$

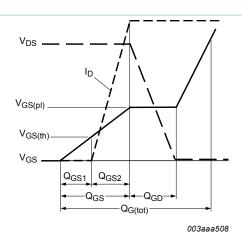


Fig. 13. Gate charge waveform definitions

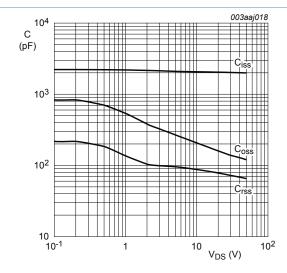


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = \mathbf{0}V; f = \mathbf{1}MHz$$

### N-channel 80 V, 27 m $\Omega$ logic level MOSFET in LFPAK56

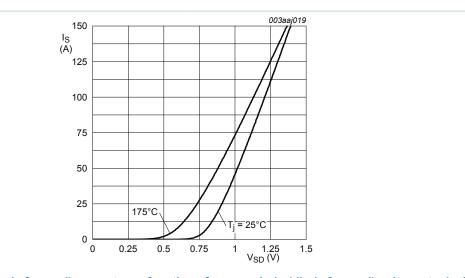


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

#### N-channel 80 V, 27 mΩ logic level MOSFET in LFPAK56

## 11. Package outline

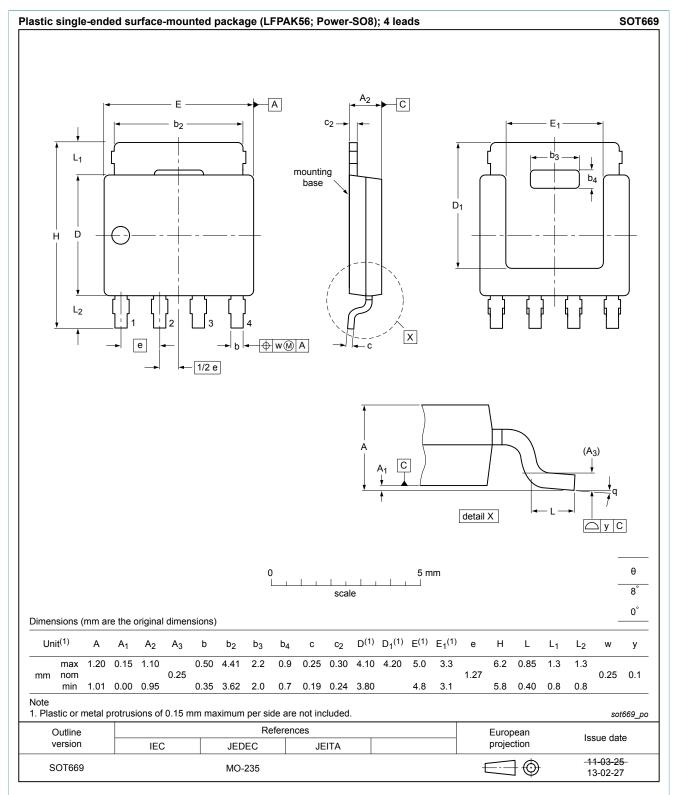


Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)

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#### N-channel 80 V, 27 mΩ logic level MOSFET in LFPAK56

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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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