

WNP 4225CP 1CFT

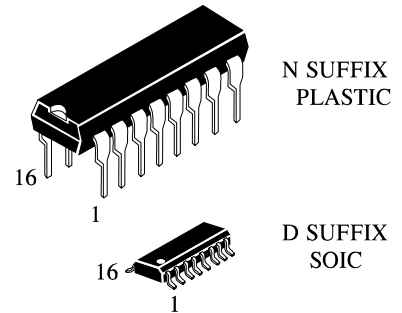


'UGXGP 'DARLINGTON' ARRAYS

The WNP 4225A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven n-p-n Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The WNP 2003A has a 2.7-k series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications



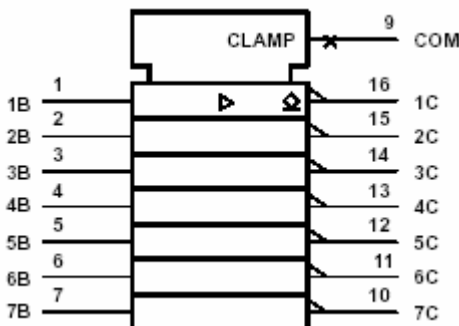
ORDERING INFORMATION

WNN2003AN "" Plastic

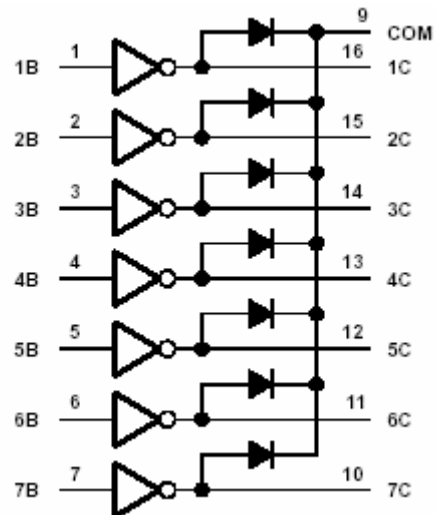
WLN2003ADT SOIC

$T_A = -20^\circ\text{C}$ to 85°C for all packages

LOGIC SYMBOL



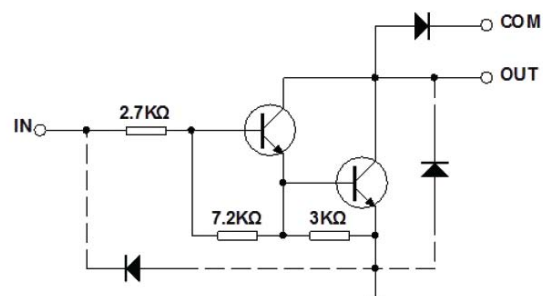
LOGIC DIAGRAM



SCHEMATICS (each Darlington Pair)

All resistor values shown are nominal.

WLN2003A: $R_B = 2.7\text{ k}\Omega$



Absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage	50 V
Input voltage, V_I (see Note 1)	30 V Peak
collector current (see Figures 14 and 15)	500 mA
Output clamp current, I_{OK}	500 mA
Total emitter-terminal current	-2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	-20°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A = 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

Electrical characteristics, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS	ULN2003A			UNIT
			MIN	TYP	MAX	
$V_{I(on)}$ On-state input voltage	6	$V_{CE} = 2\text{ V}$	$I_C = 125\text{ mA}$			V
			$I_C = 200\text{ mA}$		2.4	
			$I_C = 250\text{ mA}$		2.7	
			$I_C = 275\text{ mA}$			
			$I_C = 300\text{ mA}$		3	
			$I_C = 350\text{ mA}$			
$V_{CE(sat)}$ Collector-emitter saturation voltage	5	$I_I = 250\text{ }\mu\text{A}$, $I_C = 100\text{ mA}$	0.9	1.1		V
		$I_I = 350\text{ }\mu\text{A}$, $I_C = 200\text{ mA}$	1	1.3		
		$I_I = 500\text{ }\mu\text{A}$, $I_C = 350\text{ mA}$	1.2	1.6		
I_{CEX} Collector cutoff current	1	$V_{CE} = 50\text{ V}$, $I_I = 0$			50	μA
	2	$V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$, $I_I = 0$, $V_I = 1\text{ V}$			100	
V_F Clamp forward voltage	8	$I_F = 350\text{ mA}$		1.7	2	V
$I_{I(off)}$ Off-state input current	3	$V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$, $I_C = 500\text{ }\mu\text{A}$	50	65		μA
I_I Input current	4	$V_I = 3.85\text{ V}$		0.93	1.35	mA
		$V_I = 5\text{ V}$				
		$V_I = 12\text{ V}$				
I_R Clamp reverse current	7	$V_R = 50\text{ V}$			50	μA
		$V_R = 50\text{ V}$, $T_A = 70^\circ\text{C}$			100	
C_i Input capacitance		$V_I = 0$, $f = 1\text{ MHz}$		15	25	pF

switching characteristics, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 9		0.25	1	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.25	1	μs
V_{OH}	High-level output voltage after switching	$V_S = 50\text{ V}$, See Figure 10 $I_O \approx 300\text{ mA}$	$V_S - 20$			mV

PARAMETER MEASUREMENT INFORMATION

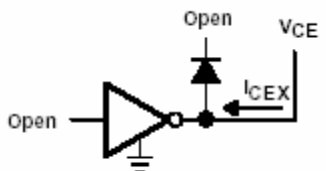


Figure 1. I_{CEX} Test Circuit

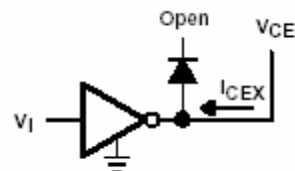


Figure 2. I_{CEX} Test Circuit

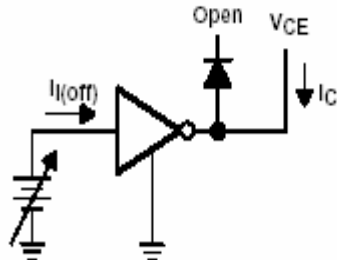


Figure 3. $I_{I(off)}$ Test Circuit

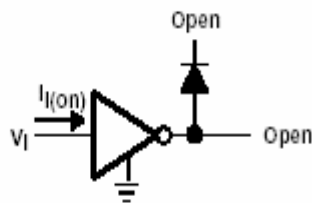
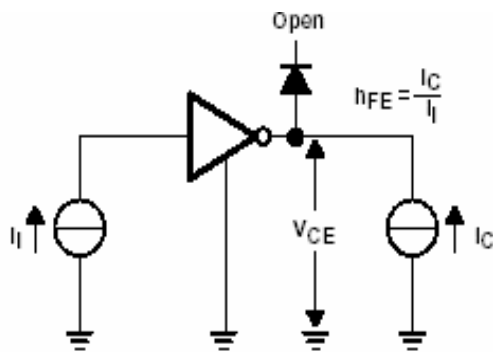


Figure 4. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE} .

Figure 5. h_{FE} , $V_{CE(sat)}$ Test Circuit

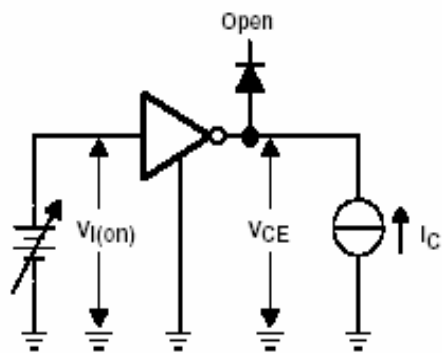


Figure 6. $V_{I(on)}$ Test Circuit

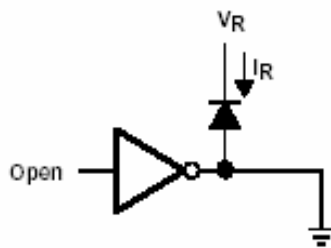


Figure 7. I_R Test Circuit

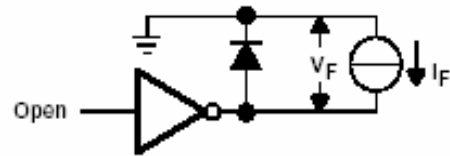


Figure 8. V_F Test Circuit

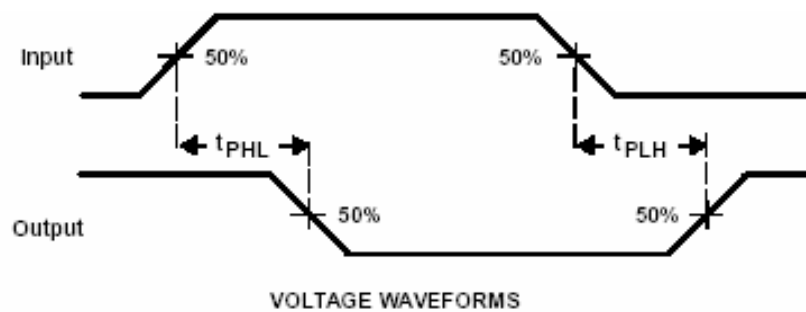
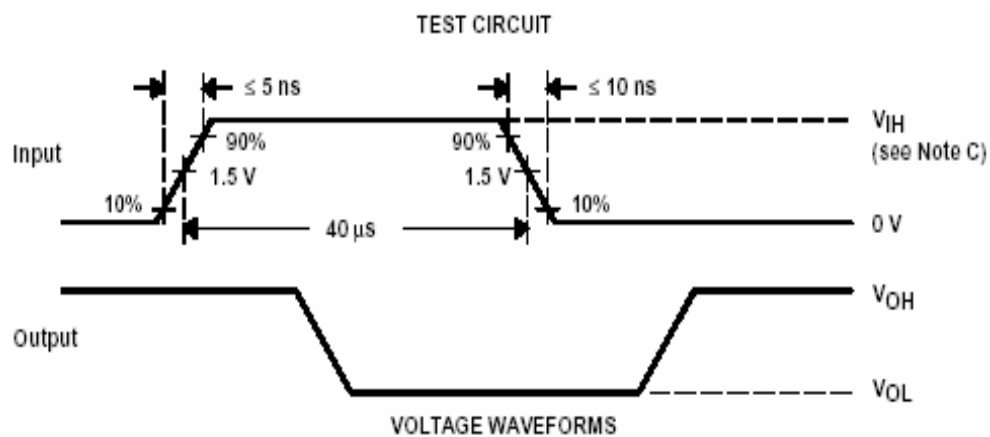


Figure 9. Propagation Delay-Time Waveforms



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_0 = 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. $V_{IH} = 3 \text{ V}$;

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

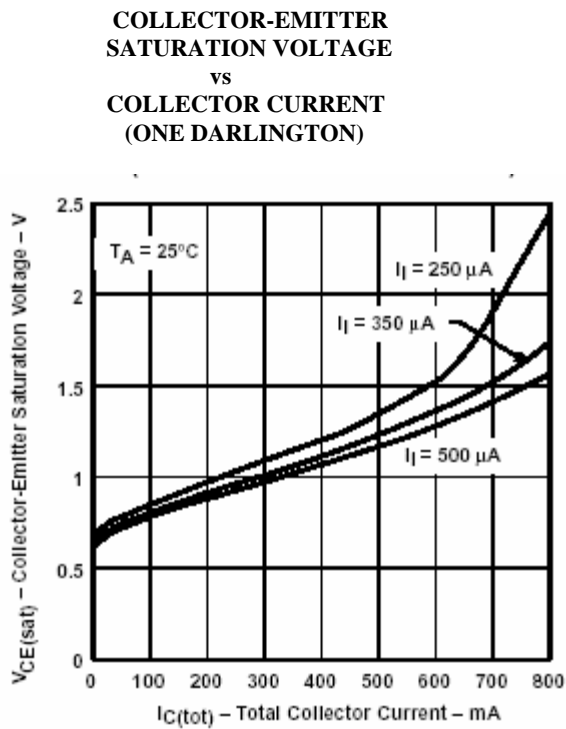


Figure 12

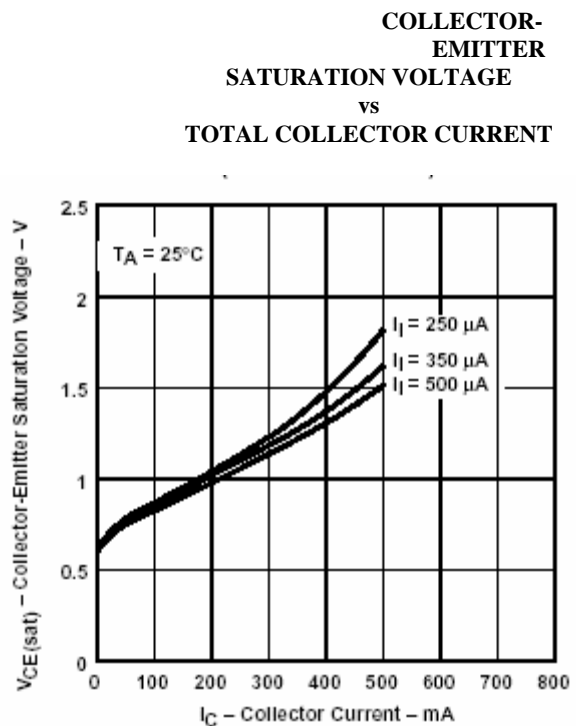


Figure 11

COLLECTOR CURRENT vs INPUT CURRENT

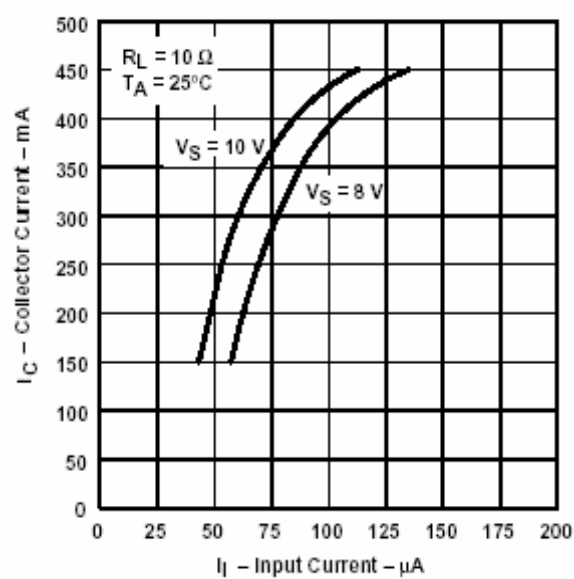


Figure 13

THERMAL INFORMATION

D PACKAGE
MAXIMUM COLLECTOR CURRENT
 V_s
DUTY CYCLE

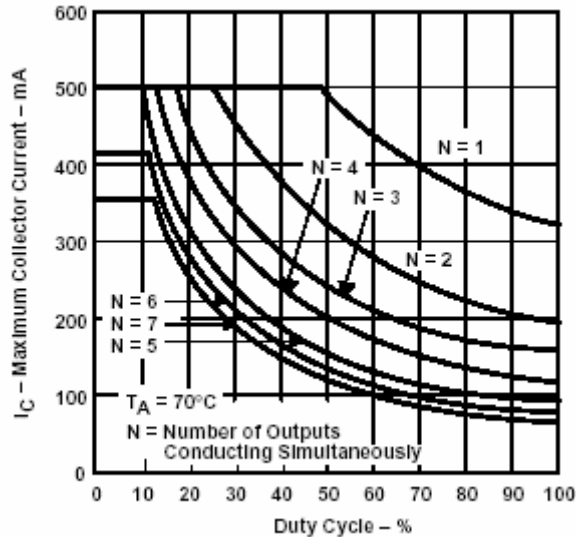


Figure 14

N PACKAGE
MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

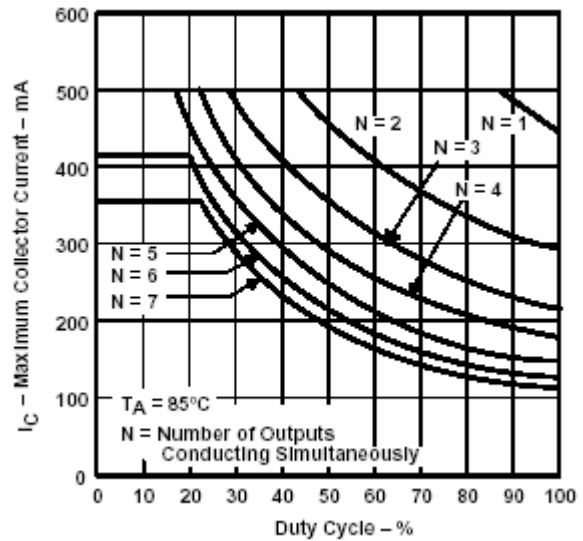


Figure 15

APPLICATION INFORMATION

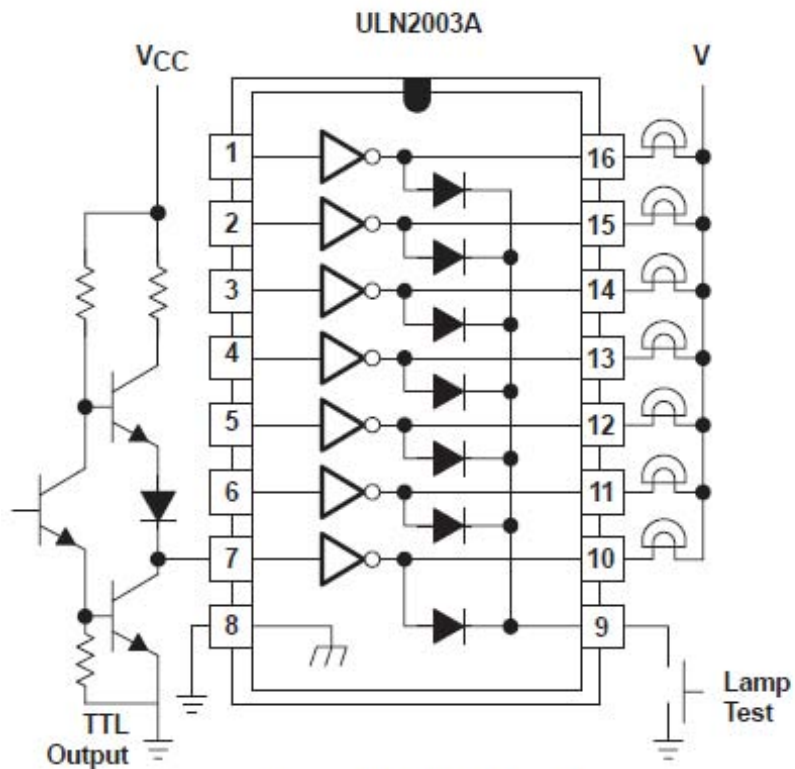


Figure 16. TTL to Load

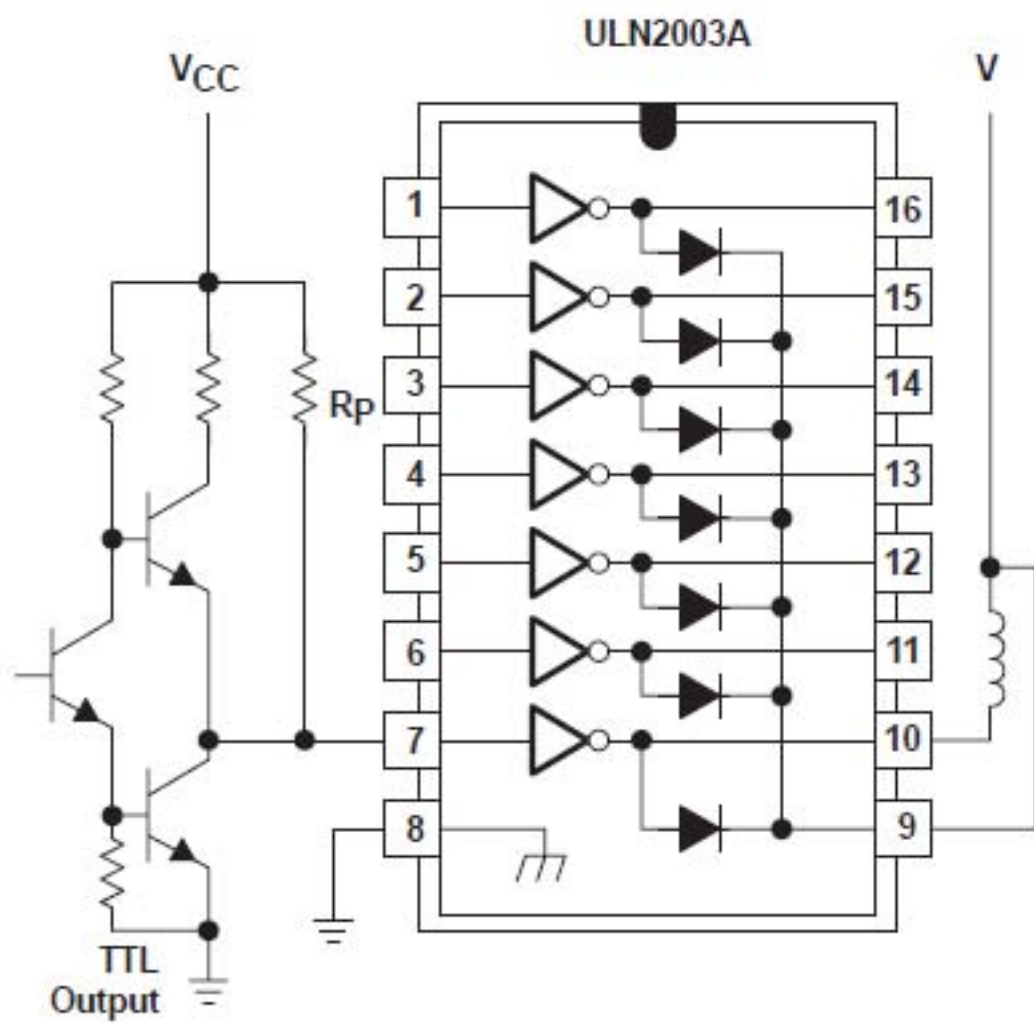
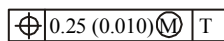
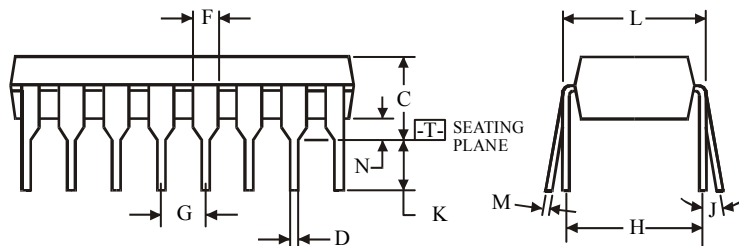
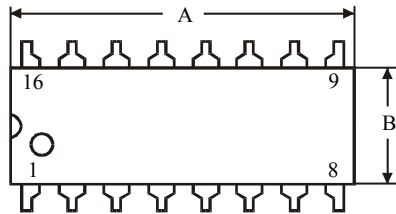


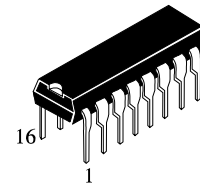
Figure 17. Use of Pullup Resistors to Increase Drive Current

**N SUFFIX PLASTIC DIP
(MS - 001BB)**



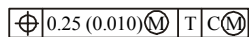
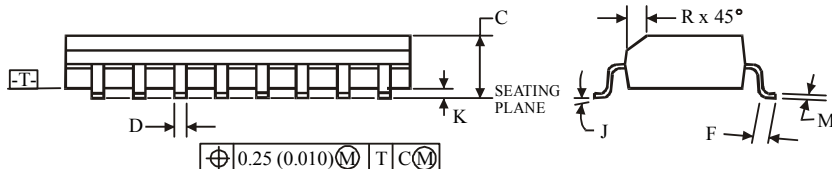
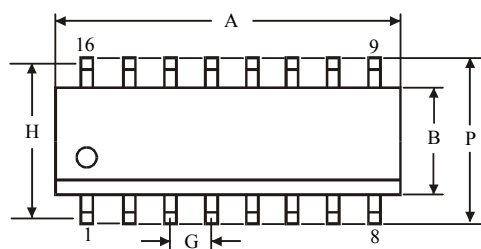
NOTES:

1. Dimensions "A", "B" do not include mold flash or protrusions.
Maximum mold flash or protrusions 0.25 mm (0.010) per side.



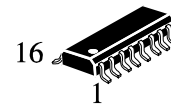
Symbol	Dimension, mm	
	MIN	MAX
A	18.67	19.69
B	6.10	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.20	0.36
N	0.38	

**D SUFFIX SOIC
(MS - 012AC)**



NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
for A; for B - 0.25 mm (0.010) per side.



Symbol	Dimension, mm	
	MIN	MAX
A	9.80	10.00
B	3.80	4.00
C	1.35	1.75
D	0.33	0.51
F	0.40	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.10	0.25
M	0.19	0.25
P	5.80	6.20
R	0.25	0.50