DUAL SYNCHRONOUS STEP-DOWN CONTROLLER FOR LOW VOLTAGE POWER RAILS

FEATURES

- **D-CAP2™ Mode Control**
  - **Fast Transient Response**
  - **No External Parts Required For Loop Compensation**
  - **Compatible with Ceramic Output Capacitors**
- **High Initial Reference Accuracy (±1%)**
- **Low Output Ripple**
- **Wide Input Voltage Range: 4.5 V to 24 V**
- **Output Voltage Range: 0.76 V to 5.5 V**
- **Low-Side $R_{DS(on)}$ Loss-Less Current Sensing**
- **Adaptive Gate Drivers with Integrated Boost Diode**
- **Internal 1.2 ms Voltage-Servo Soft Start**
- **Pre-Biased Soft Start**
- **Selectable Switching Frequency: 350 kHz / 700 kHz**
- **Cycle-by-Cycle Over-Current Limiting Control**
- **30 mV to 300 mV OCP Threshold Voltage**
- **Thermally Compensated OCP by 4000 ppm/C° at I_{TRIP}**

APPLICATIONS

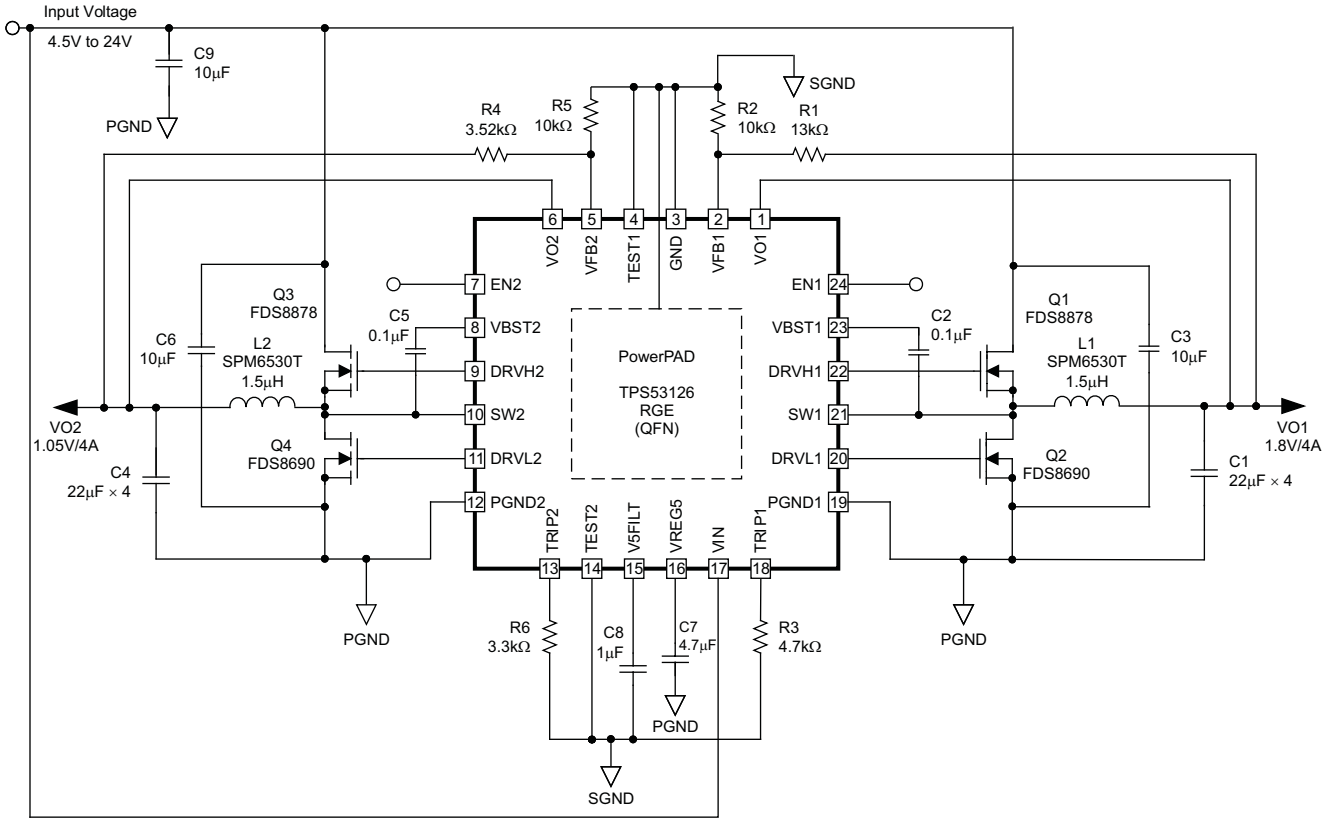
- **Point-of-Load Regulation in Low Power Systems for Wide Range of Applications**
  - **Digital TV Power Supply**
  - **Networking Home Terminal**
  - **Digital Set Top Box (STB)**
  - **DVD Player/Recorder**
  - **Gaming Consoles and Other**

DESCRIPTION

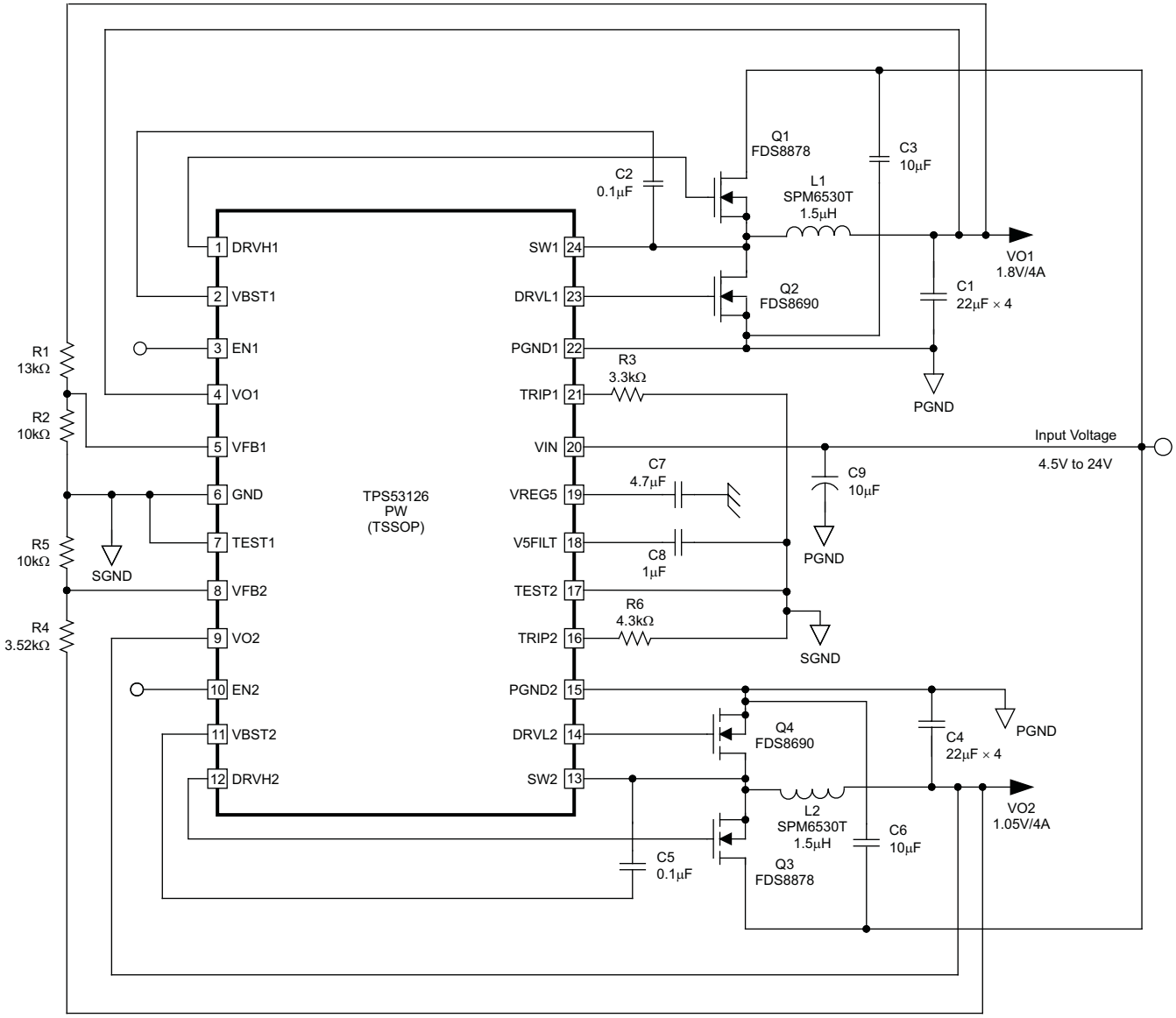
The TPS53126 is a dual, adaptive on-time, D-CAP2™ mode synchronous Buck controller. The TPS53126 enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low external component count, and low standby current solution. The main control loop for the TPS53126 uses the D-CAP2™ mode control which provides a very fast transient response with no external components. The TPS53126 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device provides convenient and efficient operation with input voltages from 4.5 V to 24 V and output voltages from 0.76 V to 5.5 V.

The TPS53126 is available in 4mm x 4mm 24 pin QFN (RGE) or 24 pin TSSOP (PW) packages and is specified from –40°C to 85°C ambient temperature range.

QFN APPLICATION DIAGRAM



TSSOP APPLICATION DIAGRAM



ORDERING INFORMATION(1)(2)

T_A	PACKAGE	ORDERING PART NUMBER	PINS	OUTPUT SUPPLY	ECO PLAN
–40°C to 85°C	Plastic Quad Flat Pack (QFN)	TPS53126RGET	24	Tape-and-Reel	Green (RoHS and no Sb/Br)
		TPS53126RGER		Tape-and-Reel	
	TSSOP	TPS53126PWR		Tape-and-Reel	
		TPS53126PW		Tube	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) All packaging options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE	UNIT
Input voltage range	VIN, EN1, EN2	–0.3 to 26	V
	VBST1, VBST2	–0.3 to 32	
	VBST1, VBST2 (wrt SWx)	–0.3 to 6	
	V5FILT, VFB1, VFB2, TRIP1, TRIP2, VO1, VO2, TEST1, TEST2	–0.3 to 6	
	SW1, SW2	–2 to 26	
Output voltage range	DRVH1, DRVH2	–1 to 32	V
	DRVH1, DRVH2 (wrt SWx)	–0.3 to 6	
	DRVL1, DRVL2, VREG5	–0.3 to 6	
	PGND1, PGND2	–0.3 to 0.3	
T_A	Operating ambient temperature range	–40 to 85	°C
T_{STG}	Storage temperature range	–55 to 150	°C
T_J	Junction temperature range	–40 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE (2 OZ. TRACE AND COPPER PAD WITH SOLDER)

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
24 pin QFN	2.33 W	23.3 mW/°C	0.93 W
24 pin TSSOP	0.778 W	7.8 mW/°C	0.31 W

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply input voltage range	VIN	4.5	24	V
	V5FILT	4.5	5.5	
Input voltage range	VBST1, VBST2	–0.1	30	V
	VBST1, VBST2 (wrt SWx)	–0.1	5.5	
	VFB1, VFB2, VO1, VO2, TEST1, TEST2	–0.1	5.5	
	TRIP1, TRIP2	–0.1	0.3	
	EN1, EN2	–0.1	24	
	SW1, SW2	–1.8	24	
Output voltage range	DRVH1, DRVH2	–0.1	30	V
	VBST1, VBST2 (wrt SWx)	–0.1	5.5	
	DRVL1, DRVL2, VREG5	–0.1	5.5	
	PGND1, PGND2	–0.1	0.1	
T_A	Operating free-air temperature	–40	85	°C
T_J	Operating junction temperature	–40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, VIN = 12 V (Unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VIN supply current	VIN current, T_A = 25°C, VREG5 tied to V5FLT, EN1 = EN2 = 5V, VFB1 = VFB2 = 0.8V, SW1 = SW2 = 0.5V		450	800	µA
I_{VINSDN}	VIN shutdown current	VIN current, T_A = 25°C, No load, EN1 = EN2 = 0 V, VREG5 = ON		30	60	µA

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, VIN = 12 V (Unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
VFB VOLTAGE and DISCHARGE RESISTANCE						
V_{BG}	Bandgap initial regulation accuracy	T_A = 25°C	-1.0%		1.0%	
$V_{VFBTHLx}$	VFBx threshold voltage	T_A = 25°C, TEST2 = 0 V, SWinj = OFF	755	765	775	mV
		T_A = –40°C to 85°C, TEST2 = 0 V, SWinj = OFF(1)	752		778	
$V_{VFBTHHx}$	VFBx threshold voltage	T_A = 25°C, TEST2 = V5FILT, SWinj = OFF	748	758	768	mV
		T_A = –40°C to 85°C, TEST2 = V5FILT, SWinj = OFF(1)	745		771	
I_{VFB}	VFB input current	VFBx = 0.8 V, T_A = 25°C		–0.01	±0.1	µA
R_{Dischg}	VO discharge resistance	ENx = 0 V, VOx = 0.5 V, T_A = 25°C		40	80	Ω
VREG5 OUTPUT						
V_{VREG5}	VREG5 output voltage	T_A = 25°C, 5.5 V < VIN < 24 V, 0 < I_{VREG5} < 10 mA	4.8	5.0	5.2	V
V_{LN5}	Line regulation	5.5 V < VIN < 24 V, I_{VREG5} = 10 mA			20	mV
V_{LD5}	Load regulation	1 mA < I_{VREG5} < 10 mA			40	mV
I_{VREG5}	Output current	VIN = 5.5 V, V_{VREG5} = 4 V, T_A = 25°C		170		mA
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVHx} = –100 mA		5.5	11	Ω
		Sink, I_{DRVHx} = 100 mA		2.5	5	
R_{DRVL}	DRVL resistance	Source, I_{DRVLx} = –100 mA		4	8	Ω
		Sink, I_{DRVLx} = 100 mA		2	4	
T_D	Dead time	DRVHx-low to DRVLx-on	20	50	80	ns
		DRVLx-low to DRVHx-on	20	40	80	
INTERNAL BOOST DIODE						
V_{FBST}	Forward voltage	$V_{VREG5-VBSTx}$, I_F = 10 mA, T_A = 25°C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST leakage current	VBSTx = 29 V, SWx = 24 V, T_A = 25°C		0.1	1	µA
ON-TIME TIMER CONTROL						
T_{ON1L}	CH1 on time	SW1 = 12 V, VO1 = 1.8 V, TEST2 = 0 V		490		ns
T_{ON2L}	CH2 on time	SW2 = 12 V, VO2 = 1.8 V, TEST2 = 0 V		390		ns
T_{OFF1L}	CH1 min off time	SW1 = 0.7 V, T_A = 25°C, VFB1 = 0.7 V, TEST2 = 0 V		285		ns
T_{OFF2L}	CH2 min off time	SW2 = 0.7 V, T_A = 25°C, VFB2 = 0.7 V, TEST2 = 0 V		285		ns
T_{ON1H}	CH1 on time	SW1 = 12 V, VO1 = 1.8 V, TEST2 = V5FILT		165		ns
T_{ON2H}	CH2 on time	SW2 = 12 V, VO2 = 1.8 V, TEST2 = V5FILT		140		ns
T_{OFF1H}	CH1 min off time	SW1 = 0.7 V, T_A = 25°C, VFB1 = 0.7 V, TEST2 = V5FILT		216		ns
T_{OFF2H}	CH2 min off time	SW2 = 0.7 V, T_A = 25°C, VFB2 = 0.7 V, TEST2 = V5FILT		216		ns
SOFT START						
T_{ss}	Internal SS time	Internal soft start VFBx = 0.735 V	0.85	1.2	1.4	ms
UVLO						
$V_{UV5VFILT}$	V5FILT UVLO threshold	Wake up	3.7	4.0	4.3	V
		Hysteresis	0.2	0.3	0.4	
LOGIC THRESHOLD						
V_{ENH}	ENx H-level input voltage	EN	2.0			V
V_{ENL}	ENx L-level input voltage	EN			0.3	V
CURRENT SENSE						
I_{TRIP}	TRIP source current	V_{TRIPx} = 0.1 V, T_A = 25°C	8.5	10	11.5	µA

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, VIN = 12 V (Unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
TC_{ITRIP}	I_{TRIP} temperature coefficient	On the basis of 25°C(2)		4000		ppm/°C
V_{OCLoff}	OCP compensation offset	($V_{TRIPx-GND}$-$V_{PGNDx-SWx}$) voltage, $V_{TRIPx-GND}$ = 60 mV, T_A = 25°C	–15	0	15	mV
		($V_{TRIPx-GND}$-$V_{PGNDx-SWx}$) voltage, $V_{TRIPx-GND}$ = 60 mV	–20		20	
V_{Rtrip}	Current limit threshold setting range	$V_{TRIPx-GND}$ voltage	30		300	mV
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	110%	115%	120%	
T_{OVPDEL}	Output OVP prop delay time			1.5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis (recovery < 20 µs)		10%		
T_{UVPDEL}	Output UVP delay time		17	30	40	µs
T_{UVPEN}	Output UVP enable delay time	UVP enable delay	1.2	2	2.5	ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(3)		150		°C
		Hysteresis(3)		20		

(2) Ensured by design. Not production tested.
(3) Ensured by design. Not production tested.

DEVICE INFORMATION

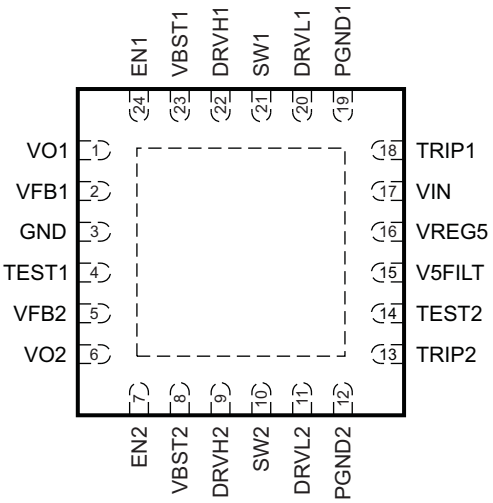
PIN FUNCTIONS

PIN			I/O	DESCRIPTION
NAME	QFN 24	TSSOP 24		
VBST1, VBST2	23, 8	2, 11	I	Supply input for high-side NFET driver (Boost Terminal). Bypass to SWx with a high-quality 0.1µF ceramic capacitor. An external schottky diode can be added if forward drop is critical to drive the high-side FET.
EN1, EN2	24, 7	3, 10	I	Channel 1 and channel 2 high level enable pins.
VO1, VO2	1, 6	4, 9	I	Output voltage inputs for on-time adjustment and output discharge. Connect directly to the output voltage.
VFB1, VFB2	2, 5	5, 8	I	D-CAP2 feedback inputs. Connect to output voltage with resistor divider.
GND	3	6	I	Signal ground pin. Connect to PGND1, PGND2 and system ground at a single point.
DRVH1, DRVH2	22, 9	1, 12	O	High-side MOSFET gate driver outputs. SWx referenced drivers switch between SWx (OFF) and VBSTx (ON).
SW1, SW2	21, 10	24, 13	I/O	Switch node connections for both the high-side drivers and the current comparators.
DRVL1, DRVL2	20, 11	23, 14	O	Low-side MOSFET gate driver outputs. PGND referenced drivers switch between PGNDx (OFF) and VREG5 (ON).
PGND1, PGND2	19, 12	22, 15	I/O	Power ground connections for both the low-side drivers and the current comparators. Connect PGND1, PGND2 and GND strongly together near the IC.
TRIP1, TRIP2	18, 13	21, 16	I	Over current trip point programming pin. Connect to GND with a resistor to GND to set threshold for low-side $R_{DS(on)}$ current limit.
VIN	17	20	I	Supply Input for 5V linear regulator.
V5FILT	15	18	I	5V supply input for the entire control circuit except the MOSFET drivers. Bypass to GND with a minimum 1.0µF, high-quality ceramic capacitor. V5FILT is connected to VREG5 via an internal 10Ω resistor.
VREG5	16	19	O	Output of 5V linear regulator and supply for MOSFET drivers. Bypass to GND with a minimum 4.7µF high-quality ceramic capacitor. VREG5 is connected to V5FILT via an internal 10Ω resistor.

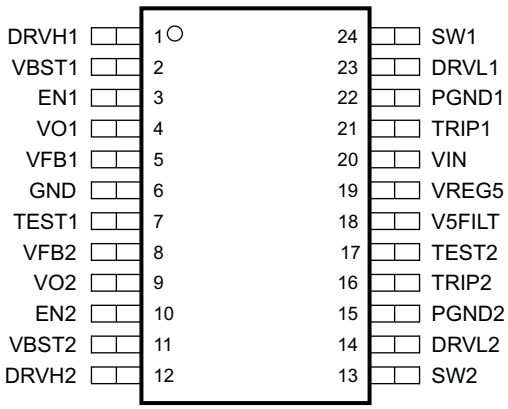
PIN FUNCTIONS (continued)

PIN			I/O	DESCRIPTION
NAME	QFN 24	TSSOP 24		
TEST1	4	7	O	Test interface pin, not used during application. Connect directly to GND.
TEST2	14	17	I	Frequency select pin. Connect to GND for 350kHz switching. Connect to V5FILT for 700kHz switching.

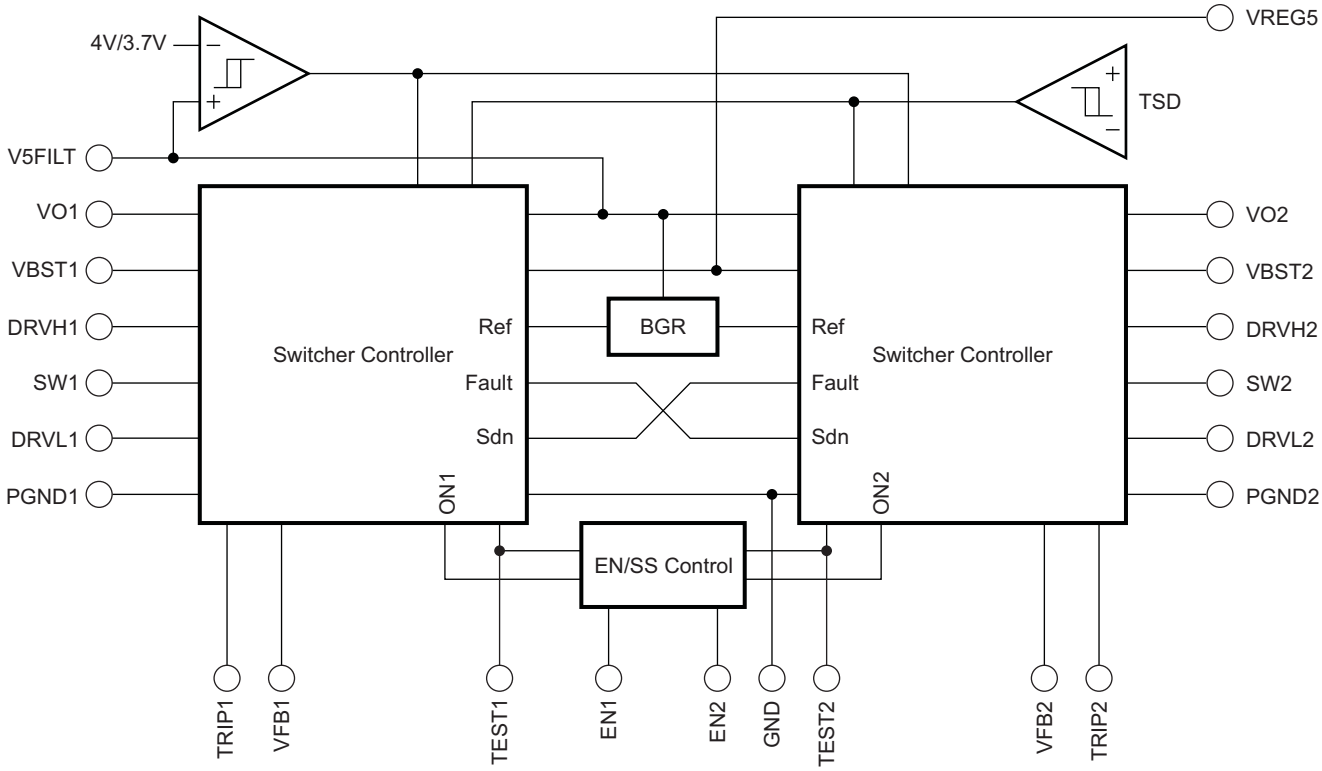
QFN (RGE) Package
(Top View)

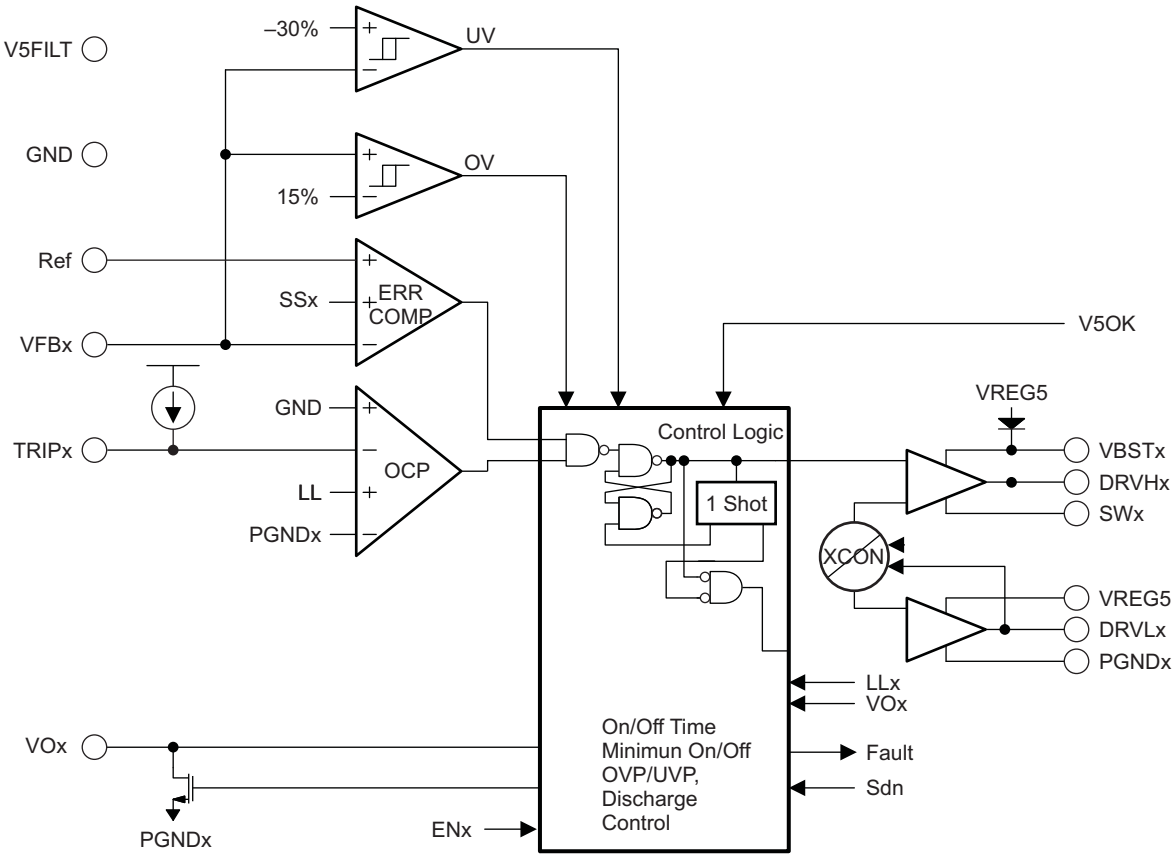


TSSOP (PW) Package
(Top View)



FUNCTIONAL BLOCK DIAGRAM





DETAILED DESCRIPTION

PWM OPERATION

The main control loop of the TPS53126 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. D-CAP2 Mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot timer is set by the converter input voltage ,VIN, and the output voltage ,VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP mode control.

DRIVERS

Each SMPS of the TPS53126 contains 2 high-current resistive MOSFET drivers. The Low-side driver is a ground referenced, VREG5 powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET whose source is connected to PGND. The High-side Driver is a floating SW referenced VBST powered driver designed to drive the gate of a high-current, low $R_{DS(on)}$ N-channel MOSFET. To maintain the BST voltage during the high-side driver ON time, a capacitor is placed from SW to VBST. Each driver draws average current equal to Gate Charge (Qg AT Vgs = 5V) times Switching Frequency (fsw).

To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFETs body diodes.

PWM FREQUENCY AND ADAPTIVE ON-TIME CONTROL

The TPS53126 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS53126 runs with pseudo-constant frequency by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

5 VOLT REGULATOR

The TPS53126 has an internal 5V Low-Dropout (LDO) Regulator to provide a regulated voltage for all four drivers and the ICs internal logic. A capacitor from VREG5 to GND is required to stabilize the internal regular. An internal 10Ω resistor from VREG5 filters the regulator output to the IC's analog and logic input voltage, V5FILT. An additional capacitor is required from V5FILT to GND to filter switching noise from VREG5.

SOFT START

The TPS53126 has an internal, 1.2ms, voltage servo soft-start for each channel. When the ENx pin becomes high, an internal DAC begins ramping up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start up. As the TPS53126 shares one DAC with both channels, if ENx pin is set to high while another channel is starting up, soft start is postponed until another channel soft start has completed. If both of EN1 and EN2 are set high at a same time, both channels start up at same time.

PRE-BIAS SUPPORT

The TPS53126 supports pre-bias start-up without sinking current from the output capacitor. When enabled, the low-side driver is held off until the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage [VFB]), then the TPS53126 slowly activates synchronous rectification by limiting the first DRVL pulses with a narrow on-time. This limited on-time is then incremented on a cycle-by-cycle basis until it coincides with the full 1-D off-time. This scheme prevents the initial sinking of current from the pre-bias output, and ensure that the output voltage (VOUT) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

SWITCHING FREQUENCY SELECTION

The TPS53126 allows the user to select from 2 different switching frequencies by connecting the TEST2 pin to either GND or V5FILT. Connect TEST2 to GND for a switching frequency (fsw) of 350KHz. Connect TEST2 to V5FILT for a switching frequency of 700KHz.

OUTPUT DISCHARGE CONTROL

The TPS53126 discharges the outputs when ENx is low, or when the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). The device discharges an output using an internal 40-Ω MOSFET which is connected to VOx and PGNDx. The external low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output. This discharge ensures that, on start, the regulated voltage always initializes from zero volts.

OVERCURRENT LIMIT

The TPS53126 has a cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET $R_{DS(on)}$ during the low-side driver on-time. If the inductor current is larger than the over current limit (OCL), the TPS53126 delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET $R_{DS(on)}$ current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, the TRIPx pin should be connected to GND through a trip voltage setting resistor, according to the following equations.

$$V_{trip} = I_{OCL} \times R_{DS(on)} - \frac{(V_{IN} - Vo)}{2 \times L1 \times fsw} \times \frac{V_O}{V_{IN}} \quad (1)$$

$$R_{trip}(k\Omega) = \frac{V_{trip}(mV)}{I_{trip}(\mu A)} \quad (2)$$

The trip voltage should be between 30mV to 300mV over all operational temperature, including the 4000ppm/°C temperature slope compensation for the temperature dependency of the $R_{DS(on)}$. If the load current exceeds the over-current limit, the voltage will begin to drop. If the over-current conditions continues the output voltage will fall below the under voltage protection threshold and the TPS53126 will shut down.

OVER/UNDER VOLTAGE PROTECTION

The TPS53126 monitors the output voltage via the feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 115% of the reference voltage, the TPS53126 turns off the high-side MOSFET driver, turns on the low-side MOSFET driver and latches off.

When the feedback voltage becomes lower than 70% of the reference voltage, the TPS53126 begins an internal UVP delay counter. After 30µs, the TPS53126 turns off both top and bottom MOSFET drivers and latches off. The UVP function is enabled approximately 2.0ms after power-on to prevent detecting UVP during soft-start. Both OVP and UVP latch conditions are reset when V5FILT triggers UVLO or the ENx pin goes low.

UVLO PROTECTION

The TPS53126 has under voltage lock out protection (UVLO) that monitors the voltage of V5FILT pin. When the V5FILT voltage is lower than UVLO threshold voltage, the device is shut off. During shut-off, VREG5 and all output drivers are OFF and output discharge is ON. The UVLO is non-latch protection.

THERMAL SHUTDOWN

The TPS53126 includes an over temperature protection shut-down feature. If the TPS53126 die temperature exceeds the OTP threshold (typically 150°C), both the high-side and low-side drivers are shut off, the output voltage discharge function is enabled and then the device is shut off until the die temperature drops. Thermal shutdown is a non-latch protection.

TYPICAL CHARACTERISTICS

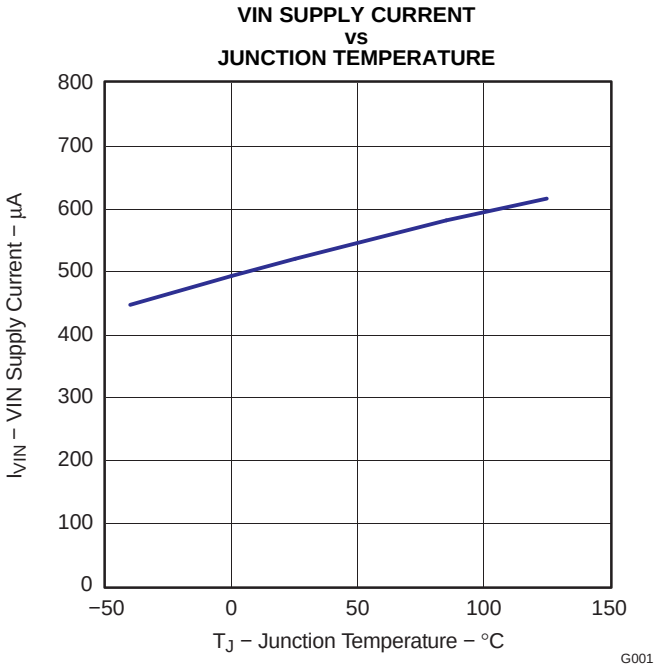


Figure 1.

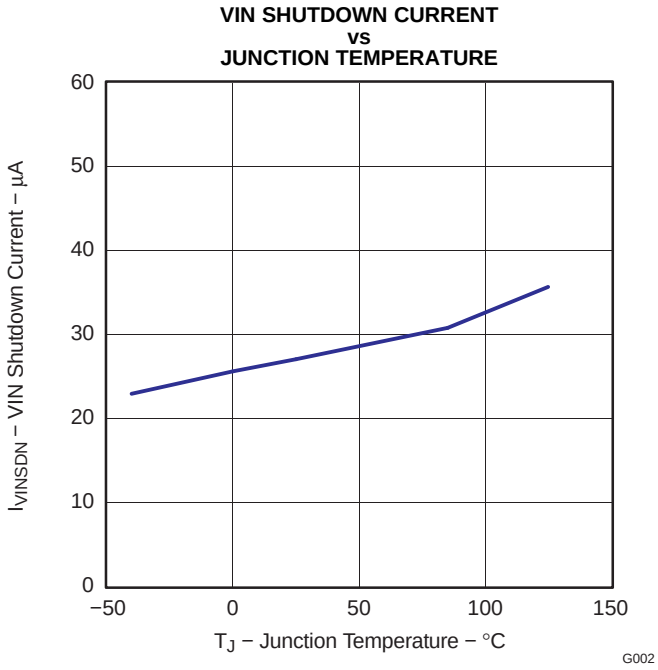


Figure 2.

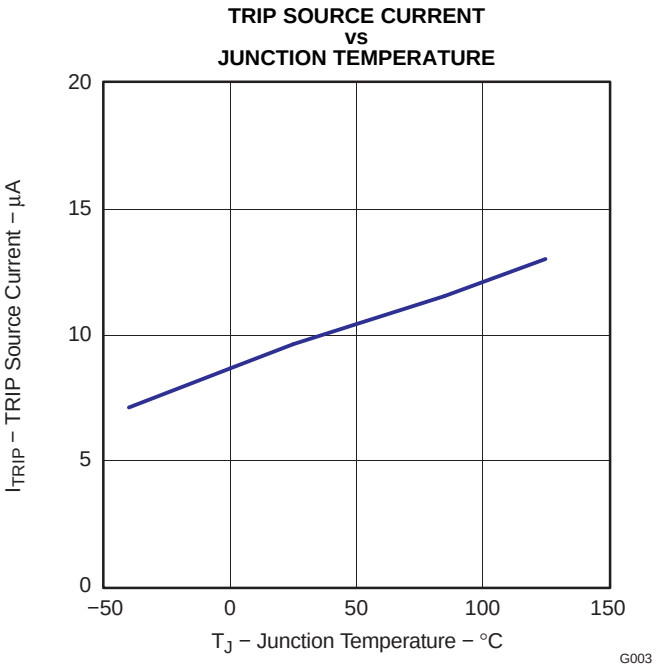


Figure 3.

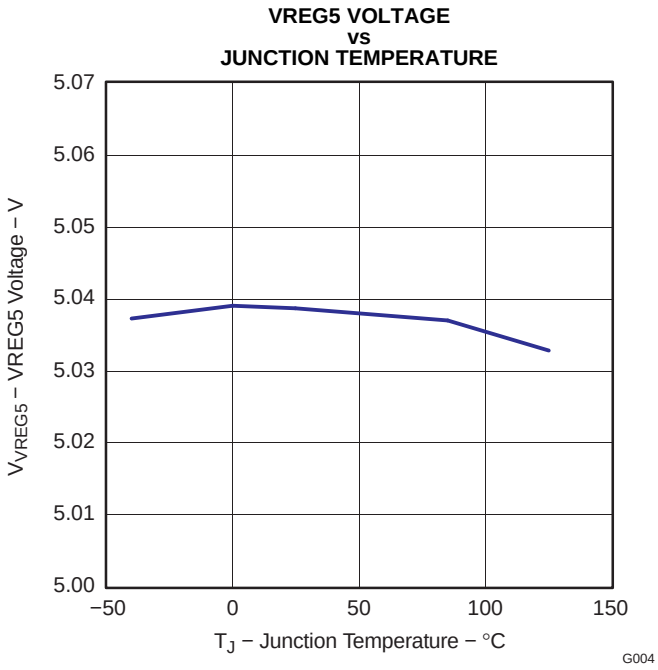


Figure 4.

TYPICAL CHARACTERISTICS (continued)

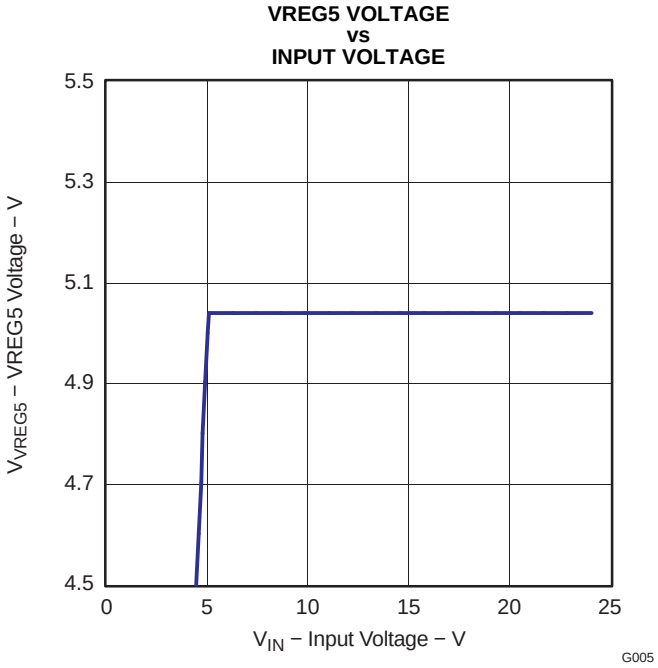


Figure 5.

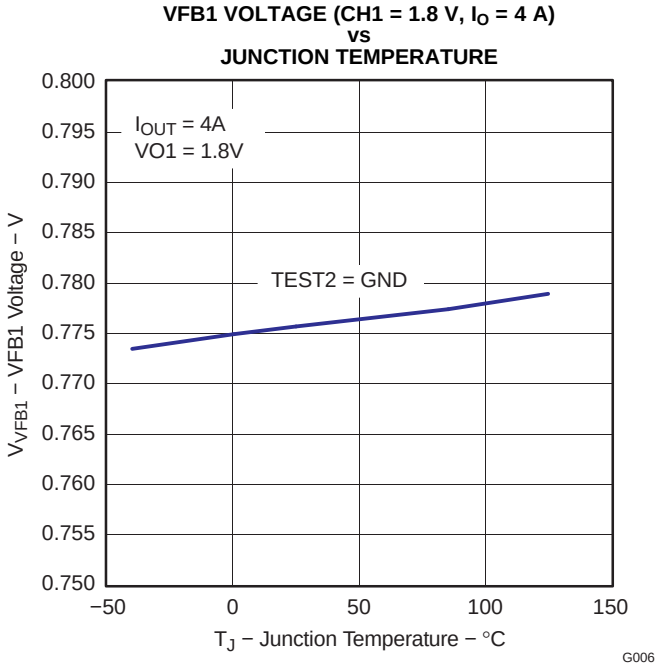


Figure 6.

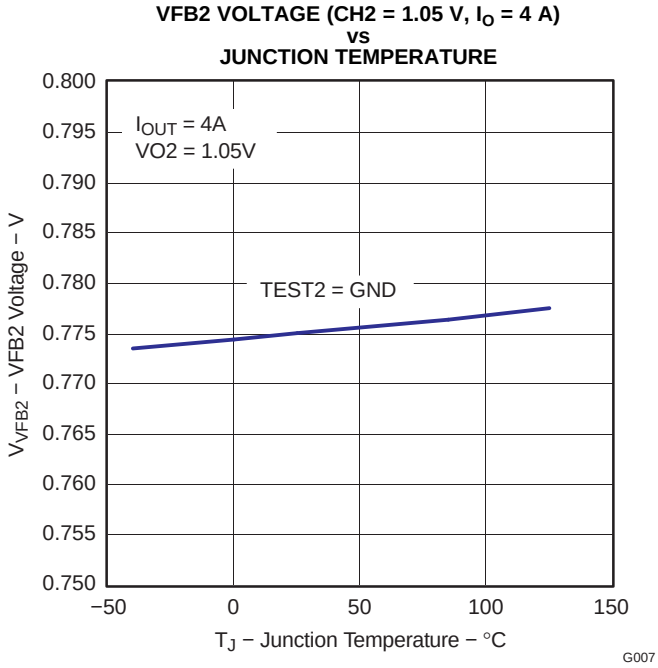


Figure 7.

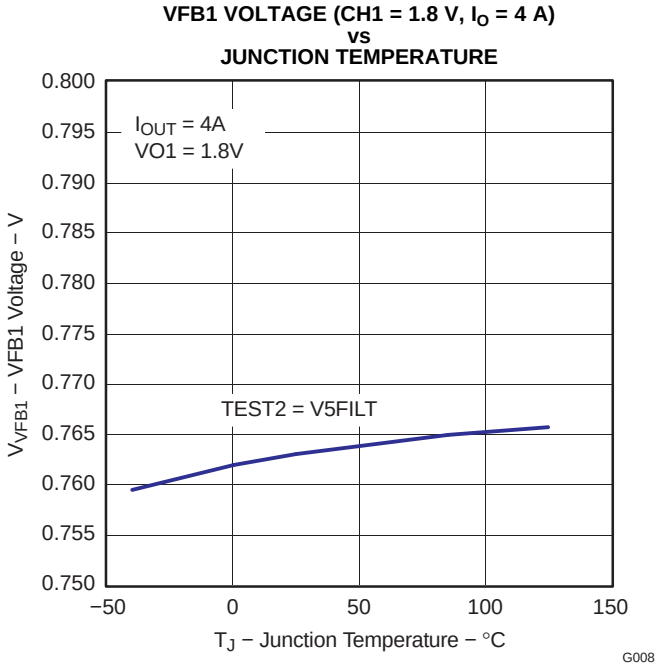


Figure 8.

TYPICAL CHARACTERISTICS (continued)

VFB2 VOLTAGE (CH2 = 1.05 V, I_O = 4 A) vs JUNCTION TEMPERATURE

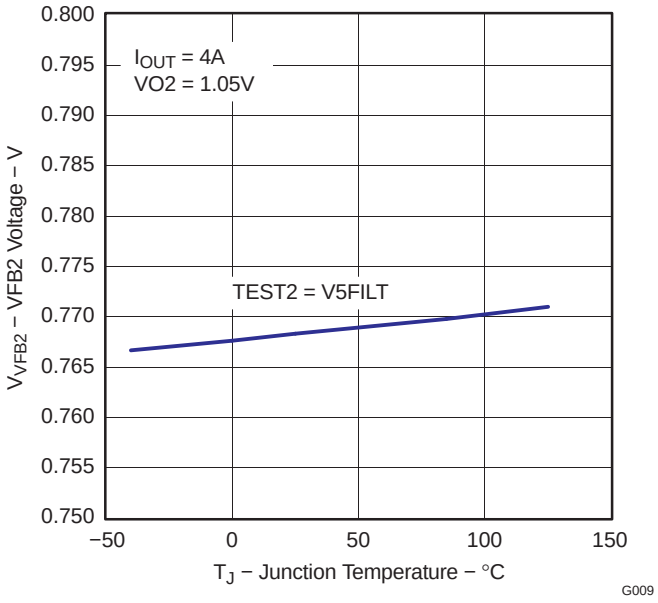


Figure 9.

VFB1 VOLTAGE (CH1 = 1.8 V) vs INPUT VOLTAGE

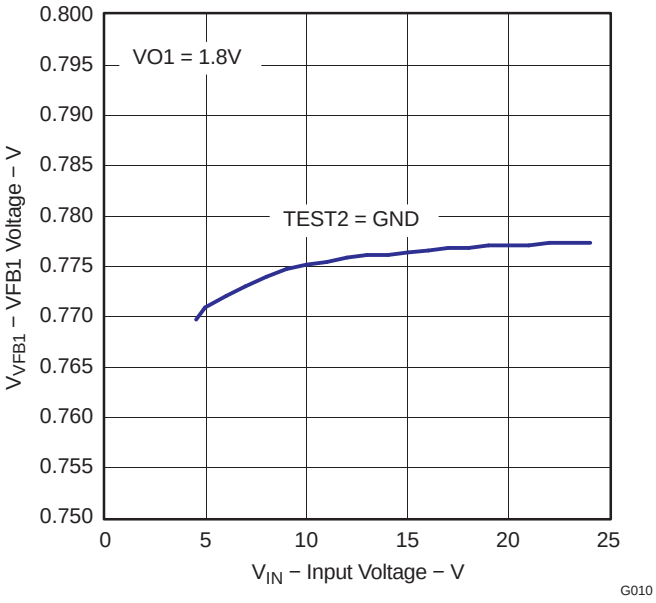


Figure 10.

VFB2 VOLTAGE (CH2 = 1.05 V) vs INPUT VOLTAGE

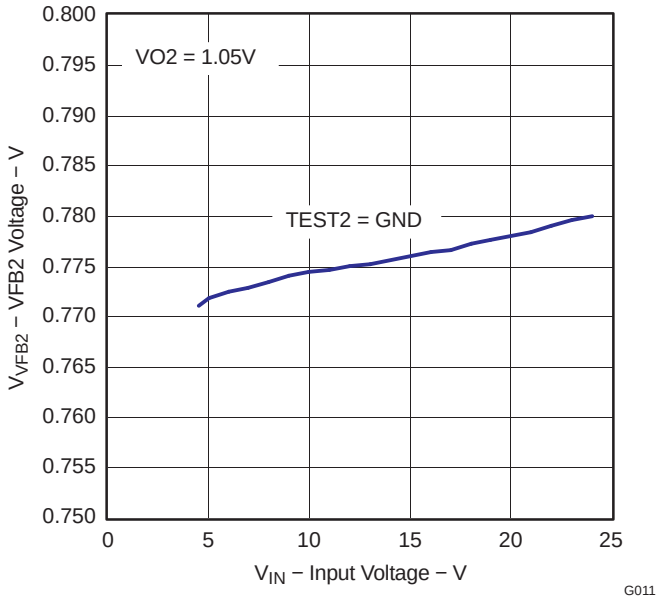


Figure 11.

VFB1 VOLTAGE (CH1 = 1.8 V) vs INPUT VOLTAGE

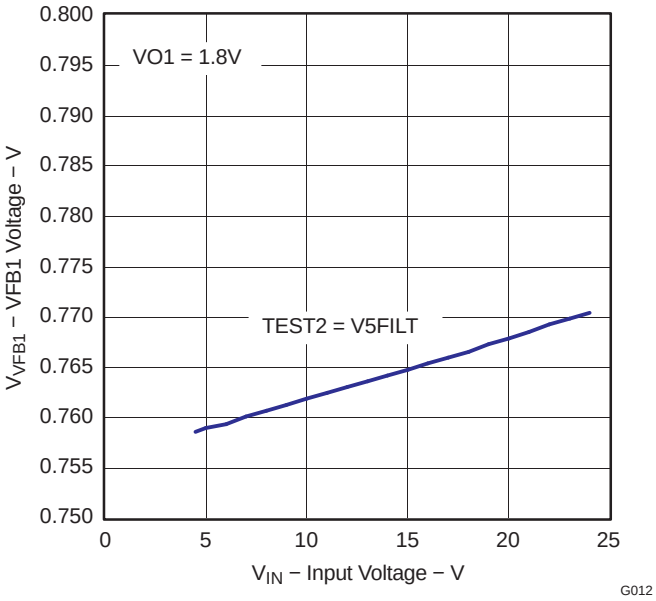


Figure 12.

TYPICAL CHARACTERISTICS (continued)

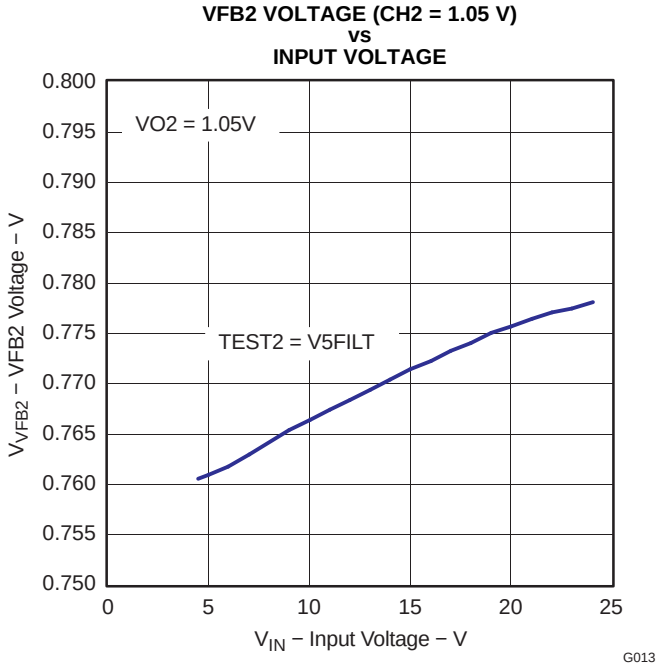


Figure 13.

TYPICAL APPLICATION PERFORMANCE

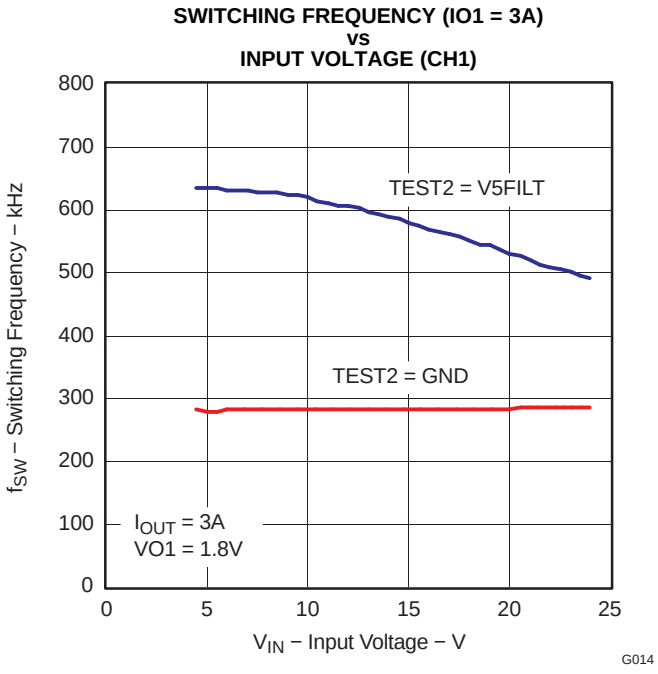


Figure 14.

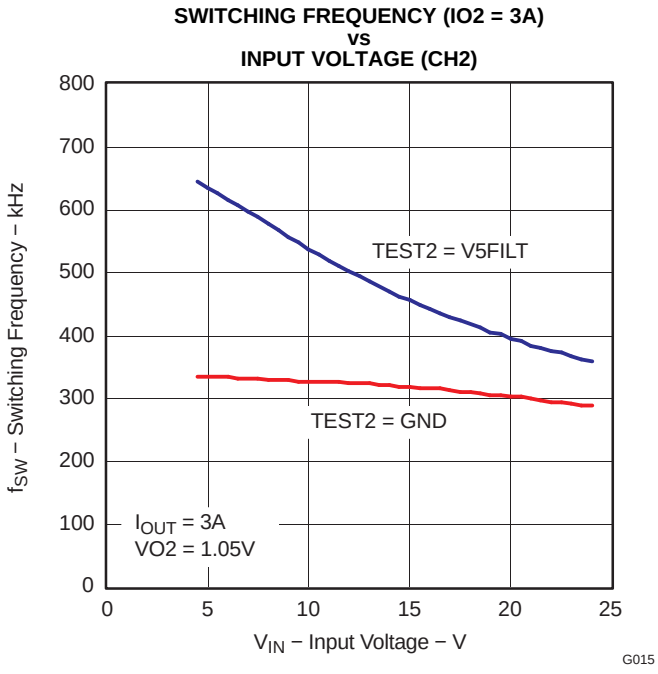


Figure 15.

TYPICAL APPLICATION PERFORMANCE (continued)

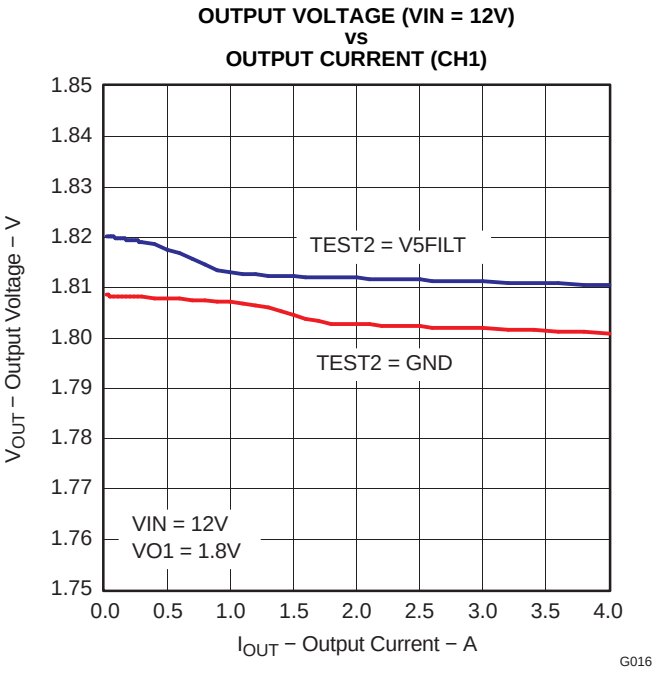


Figure 16.

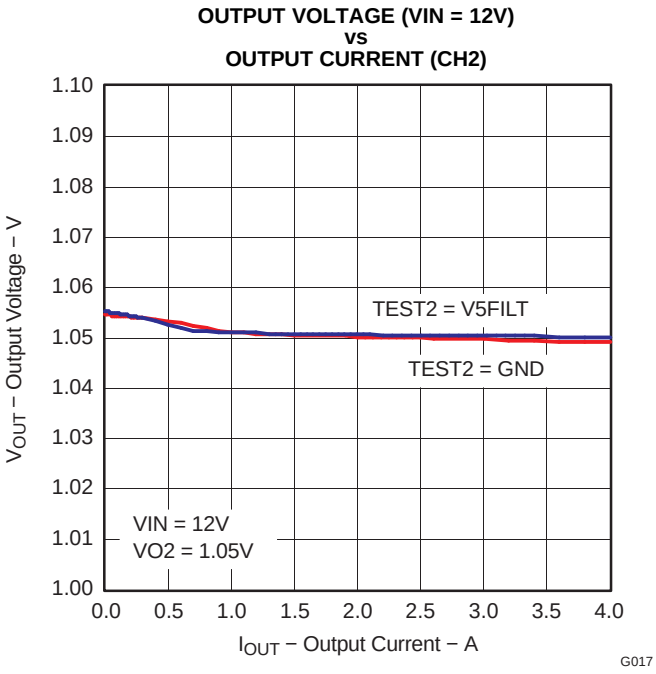


Figure 17.

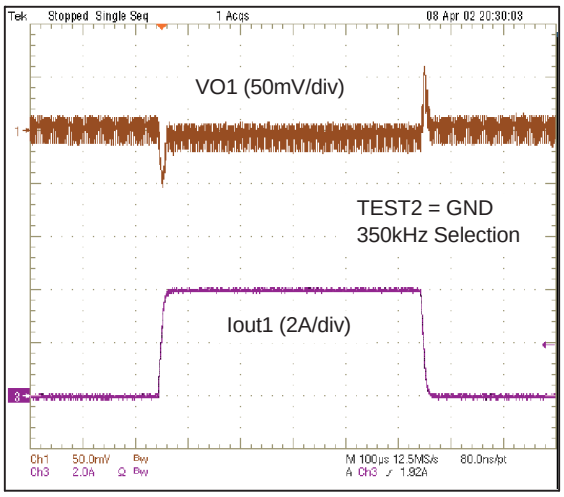


Figure 18. 1.8V LOAD TRANSIENT RESPONSE (CH1,TEST2 = GND)

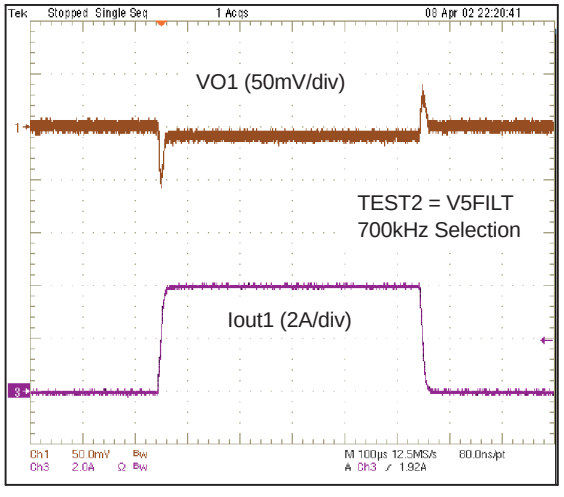
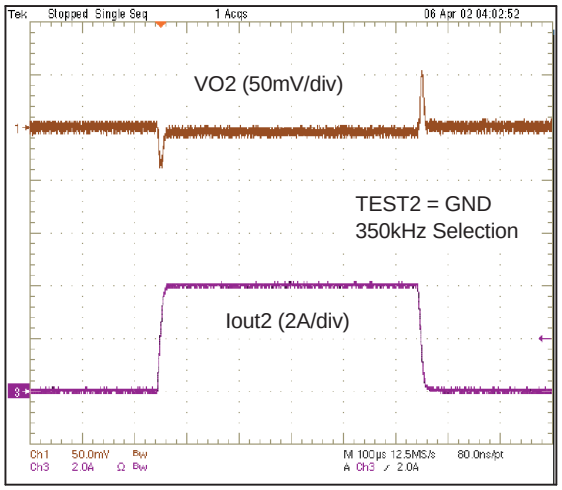


Figure 19. 1.8V LOAD TRANSIENT RESPONSE (CH1,TEST2 = V5FILT)

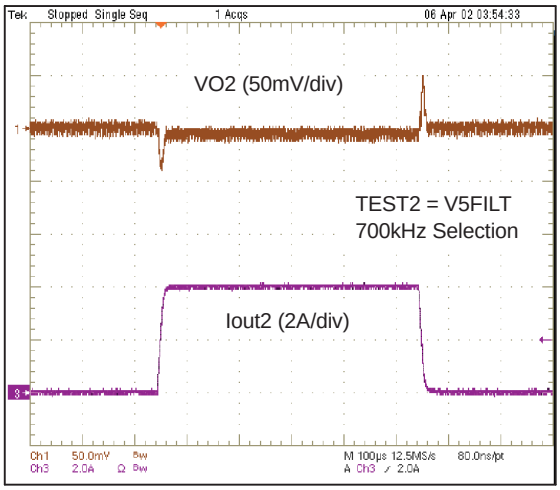
TYPICAL APPLICATION PERFORMANCE (continued)



t − time − 100µs/div C_{OUT} = 22µF × 4

G020

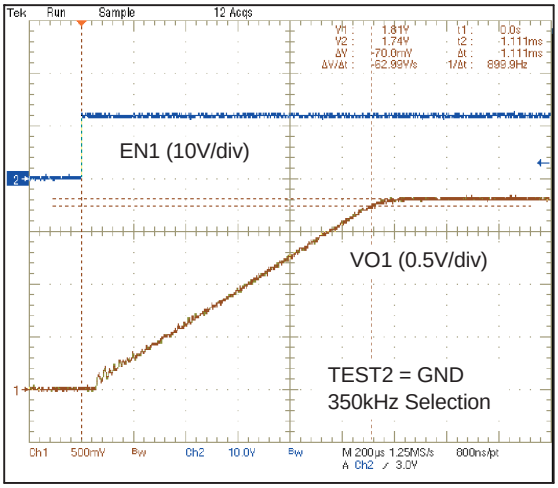
Figure 20. 1.05V LOAD TRANSIENT RESPONSE (CH2,TEST2 = V5FILT)



t − time − 100µs/div C_{OUT} = 22µF × 2

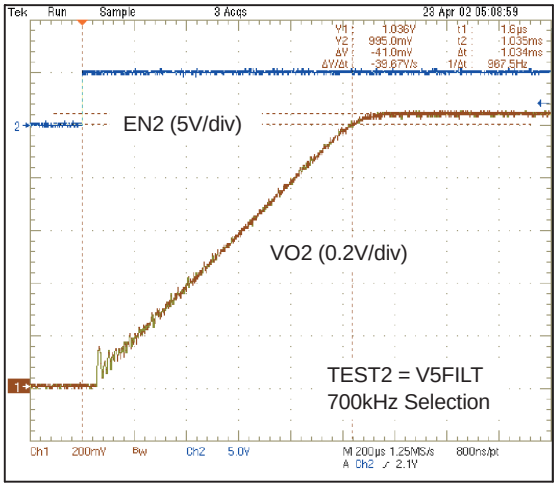
G021

Figure 21. 1.05V LOAD TRANSIENT RESPONSE (CH2,TEST2 = V5FILT)



G022

Figure 22. 1.8V START-UP WAVEFORMS



G023

Figure 23. 1.05V START-UP WAVEFORMS

TYPICAL APPLICATION PERFORMANCE (continued)

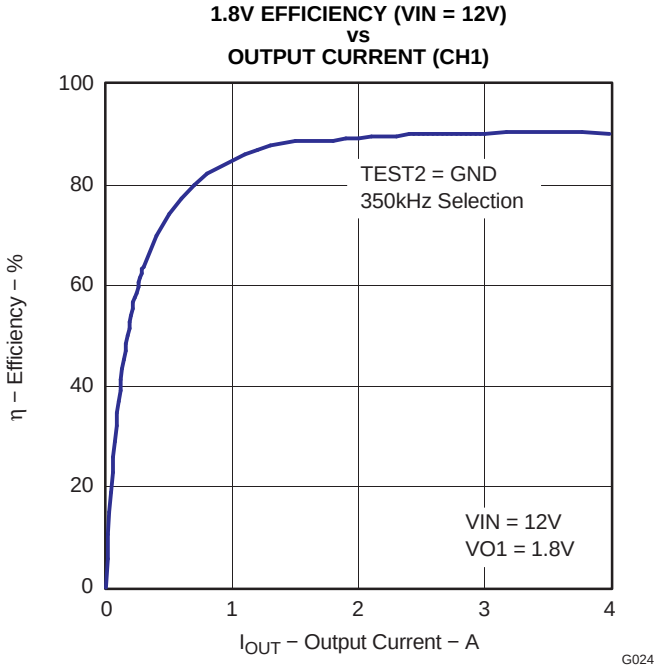


Figure 24.

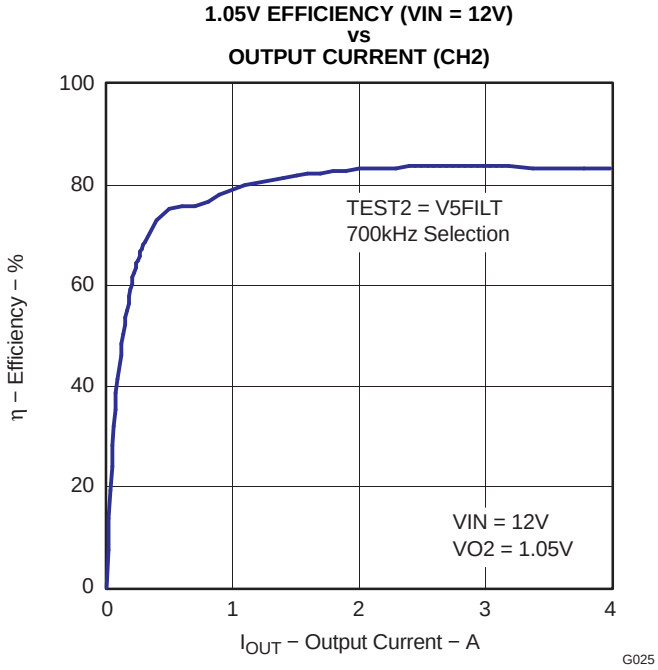


Figure 25.

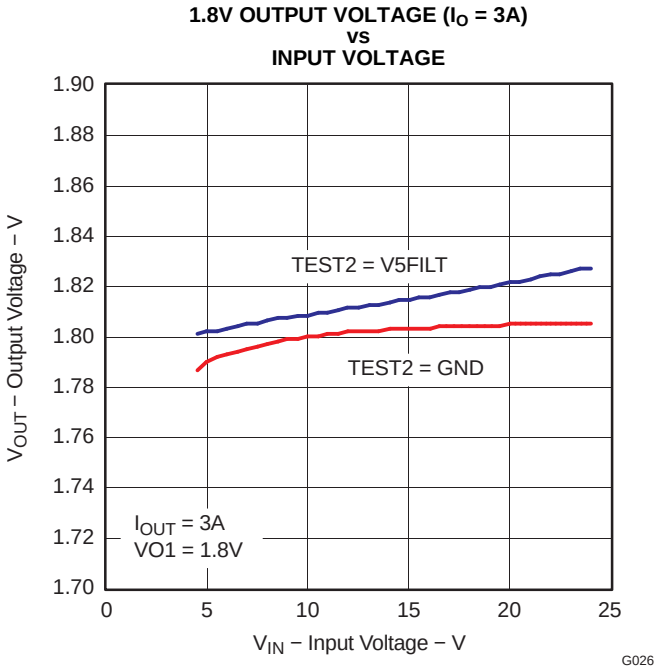


Figure 26.

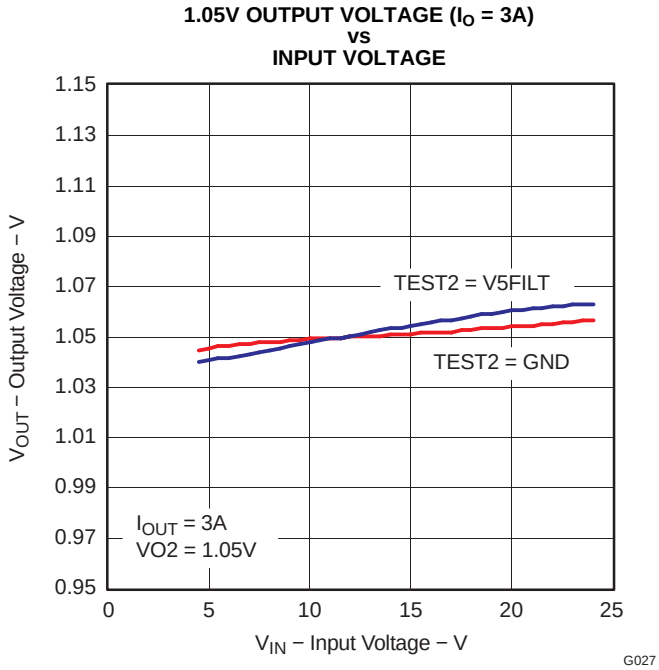


Figure 27.

TYPICAL APPLICATION PERFORMANCE (continued)

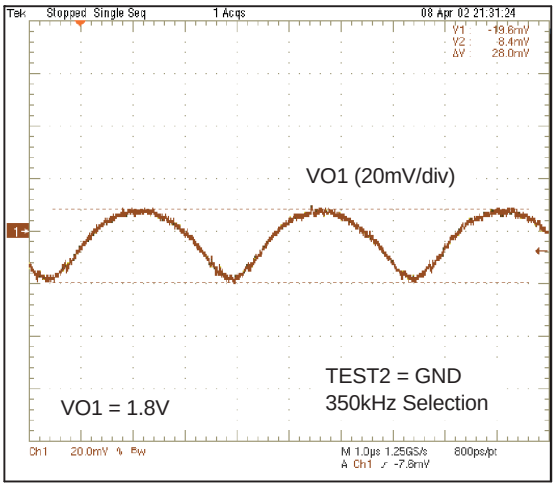


Figure 28. 1.8V OUTPUT RIPPLE VOLTAGE

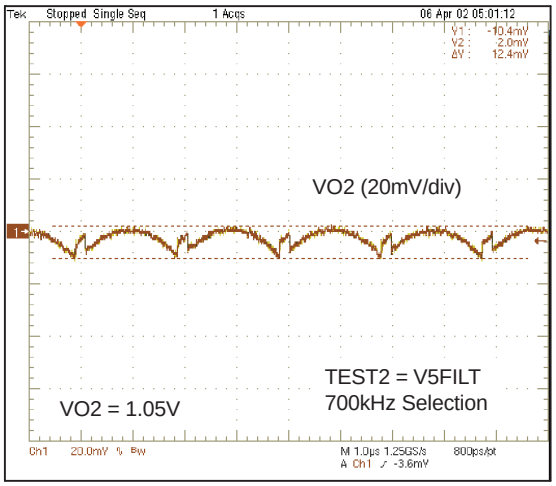


Figure 29. 1.05V OUTPUT RIPPLE VOLTAGE

APPLICATION INFORMATION

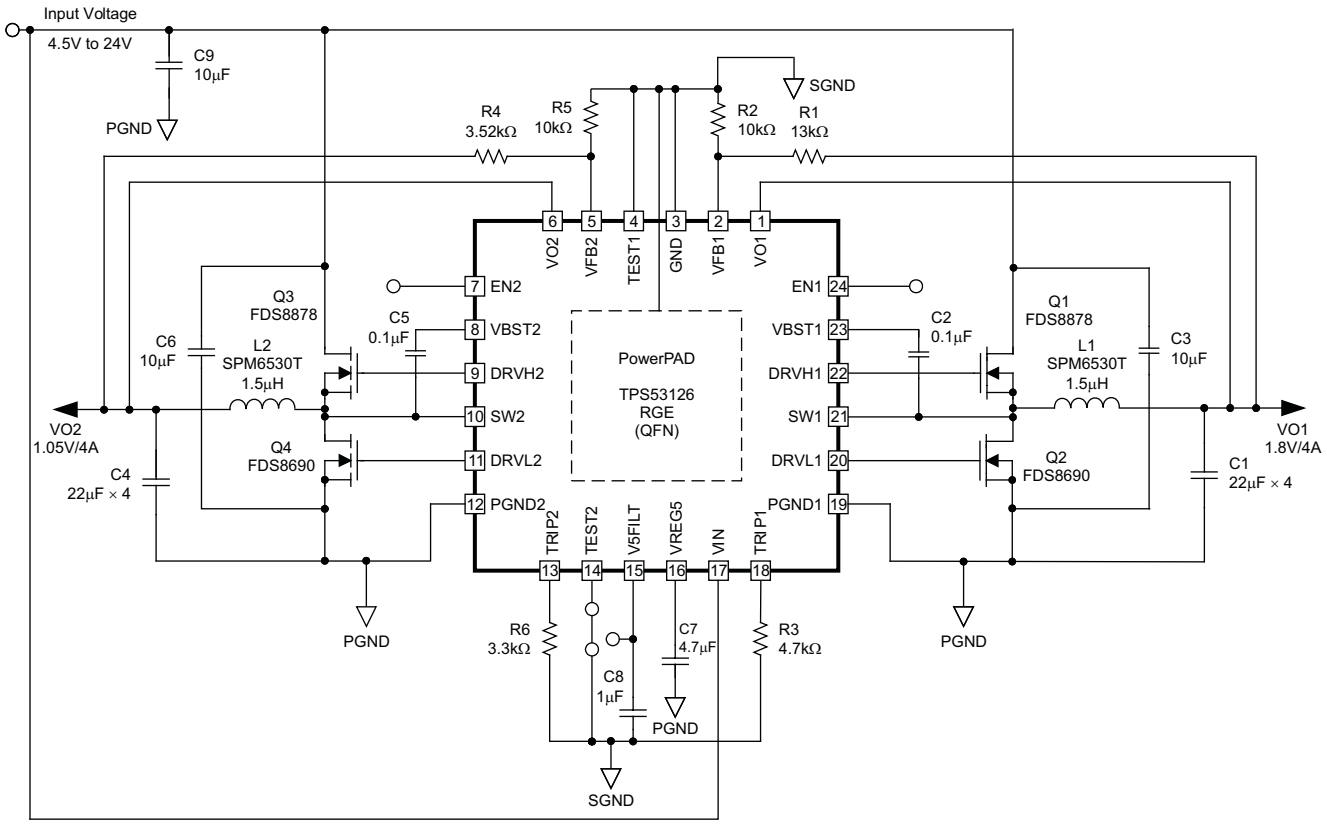


Figure 30. Typical Application Circuit at 350kHz Switching Frequency Selection (TEST2 Pin = GND)

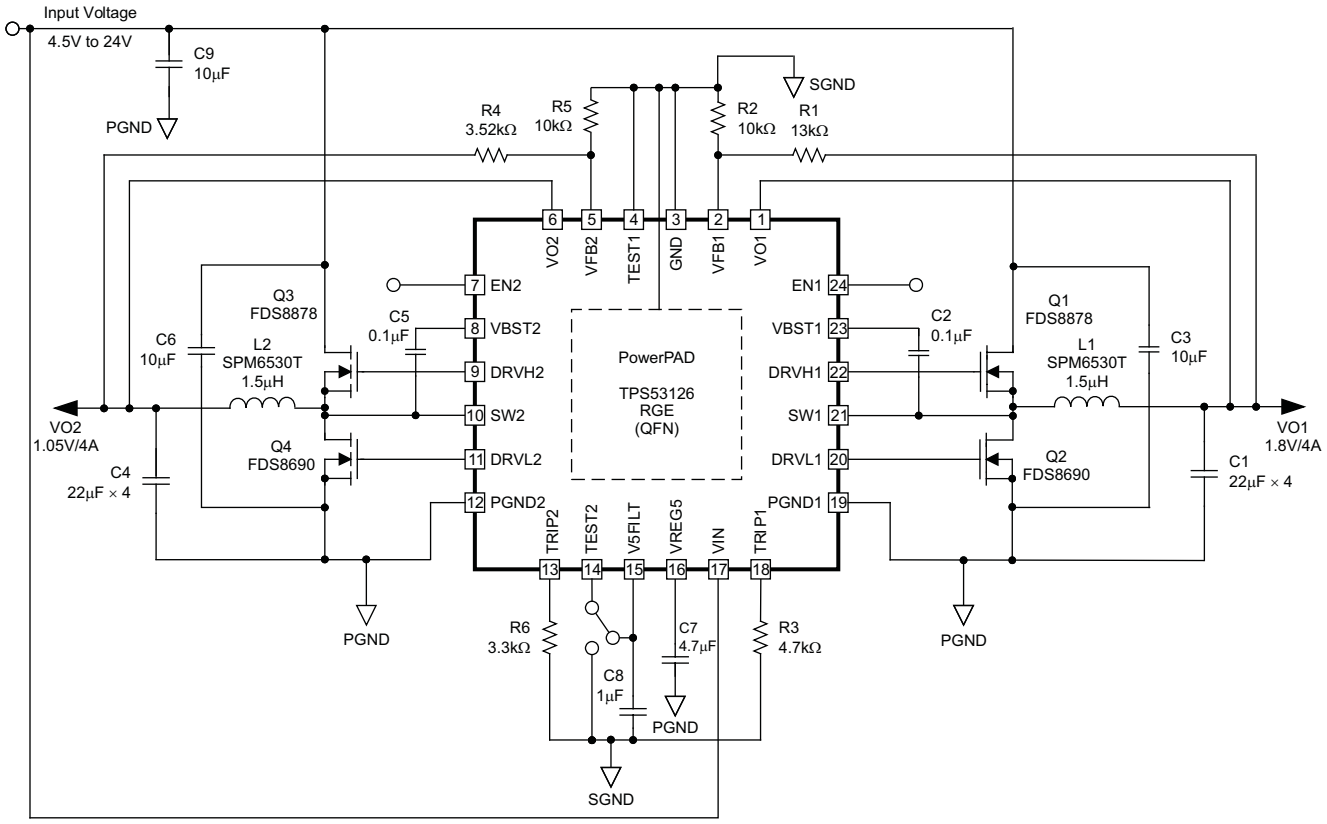


Figure 31. Typical Application Circuit at 700 kHz Switching frequency Selection (TEST2 Pin = V5FILT)

Component Selection:

1. Choose inductor.

   The inductance value is selected to provide approximately 30% peak to peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improve S/N ratio and contribute to stable operation. Equation 3 can be used to calculate L1.

$$L1 = \frac{\left(V_{IN(max)} - Vo1\right)}{I_{L1(ripple)} \times fsw} \times \frac{Vo1}{V_{IN(max)}} = \frac{3 \times \left(V_{IN(max)} - Vo1\right)}{Io1 \times fsw} \times \frac{Vo1}{V_{IN(max)}} \quad (3)$$

   The inductors current ratings needs to support both the RMS (thermal) current and the Peak (saturation) current. The RMS and peak inductor current can be estimated as follows:

$$I_{L1(ripple)} = \frac{V_{IN(max)} - Vo1}{L1 \times fsw} \times \frac{Vo1}{V_{IN(max)}} \quad (4)$$

$$I_{L1(peak)} = \frac{V_{trip}}{R_{DS(on)}} + I_{L1(ripple)} \quad (5)$$

$$I_{L1(RMS)} = \sqrt{Io1^2 + \frac{1}{12}\left(I_{L1(ripple)}\right)^2} \quad (6)$$

   Note: The calculation above shall serve as a general reference. To further improve transient response, the output inductance could be reduced further. This needs to be considered along with the selection of the output capacitor.

2. Choose output capacitor.

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. Recommend to use ceramic output capacitor.

$$C1 = \frac{\Delta Iload^2 \times L1}{2 \times Vo1 \times \Delta Vos} \quad (7)$$

$$C1 = \frac{\Delta Iload^2 \times L1}{2 \times K \times \Delta Vus} \quad (8)$$

Where:

$$K = \left((V_{IN} - Vo1) - \frac{Tmin(off)}{Ton1} \times Vo1 \right) \times \frac{Ton1}{Ton1 + Tmin(off)} \quad (9)$$

$$C1 = \frac{I_{L1(ripple)}}{8 \ Vo1(ripple)} \times \frac{1}{fsw} \quad (10)$$

Select the capacitance value greater than the largest value calculated from Equation 7, Equation 8 and Equation 10. The capacitance for C1 should be greater than 66 µF.

Where:
ΔVos = the allowable amount of overshoot voltage in load transition
ΔVus = the allowable amount of undershoot voltage in load transition
Tmin(off) = Min-off time

3. Choose input capacitor.

   The TPS53126 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10-µF high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

4. Choose bootstrap capacitor.

   The TPS53126 requires a bootstrap capacitor from SWx to VBSTx to provide the floating supply for the high-side drivers. A minimum 0.1-µF high-quality ceramic capacitor is recommended. The voltage rating should be greater than 6 V.

5. Choose VREG5 and V5FILT capacitors.

   The TPS53126 requires both the VREG5 regulator and V5FILT input are bypassed. A minimum 4.7-µF high-quality ceramic capacitor must be connected between the VREG5 and GND for proper operation. A minimum 1.0-µF high-quality ceramic capacitor must be connected between the V5FILT and GND for proper operation. Both of these capacitors' voltage ratings should be greater than 6 V.

6. Choose output voltage divide resistors.

   The output voltage is set with a resistor divider from output voltage node to the VFBx pin. It is recommended to use 1% tolerance or better resisters. Select R2 between 10 kΩ and 100 kΩ and use Equation 11 and Equation 12 to calculate R1.

$$R1 = \left(\frac{Vo1}{0.765 + \frac{VFB1_{(ripple)}}{2}} - 1 \right) \times R2 \qquad (TEST2=GND) \quad (11)$$

$$R1 = \left(\frac{Vo1}{0.758 + \frac{VFB1_{(ripple)}}{2}} - 1 \right) \times R2 \qquad (TEST2 = V5FILT) \quad (12)$$

Where:

$VFB1_{(ripple)}$ = Ripple Voltage at VFB1

7. Choose resister setting for over current limit.

$$V_{trip} = \left(I_{OCL} + \frac{(V_{IN} - Vo)}{2 \times L1 \times fsw} \times \frac{V_O}{V_{IN}} \right) \times R_{DS(on)} \quad (13)$$

$$R_{trip}(k\Omega) = \frac{V_{trip}(mV)}{I_{trip}(\mu A)} \quad (14)$$

Where:

$R_{DS(on)}$ = Low Side FET on-resistance
I_{trip} = TRIP pin source current （= 10 μA）
I_{OCL} = Over current limit

LAYOUT SUGGESTIONS

- **Keep the input switching current loop as small as possible.**
- **Place the input capacitor (C3,C6) close to the top switching FET. The output current loop should also be kept as small as possible.**
- **Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions Kelvin connections should be brought from the output to the feedback pin (FBx) of the device.**
- **Keep analog and non-switching components away from switching components**
- **Make a single point connection from the signal ground to power ground**
- **Do not allow switching current to flow under the device**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS53126PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS53126PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS53126RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS53126RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

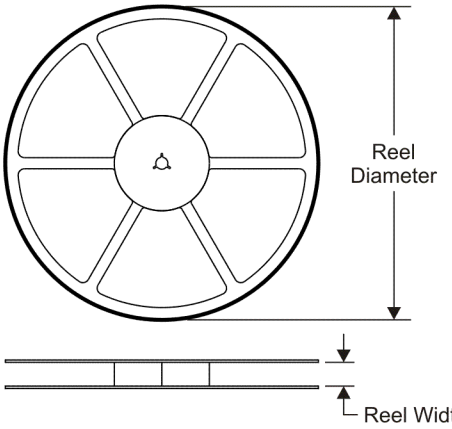
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

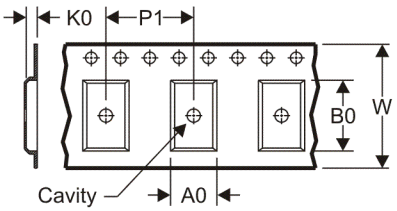
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

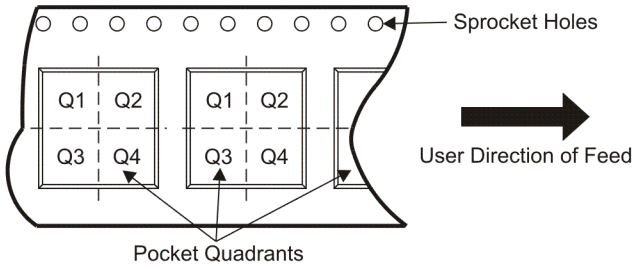


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

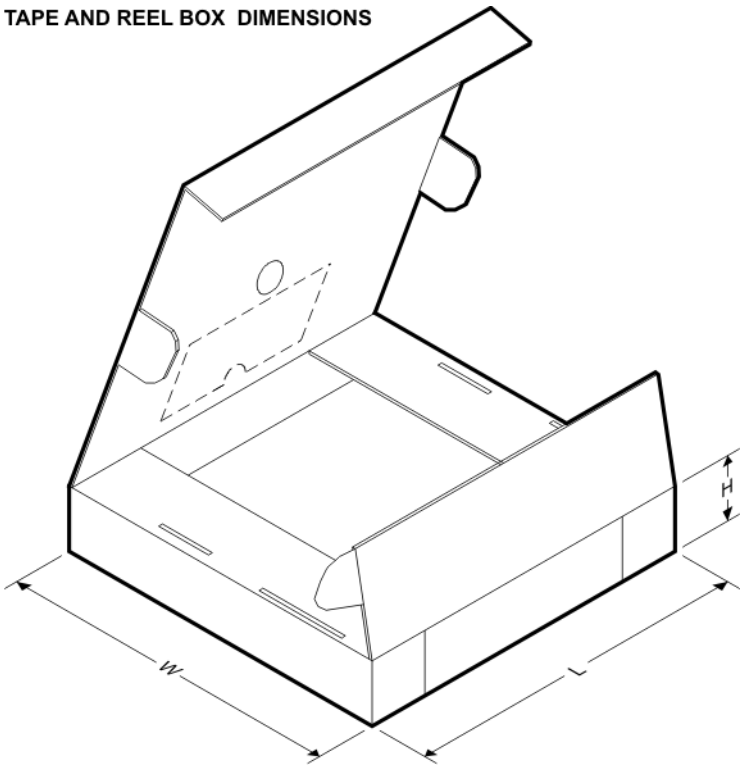
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53126PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS53126RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS53126RGET	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

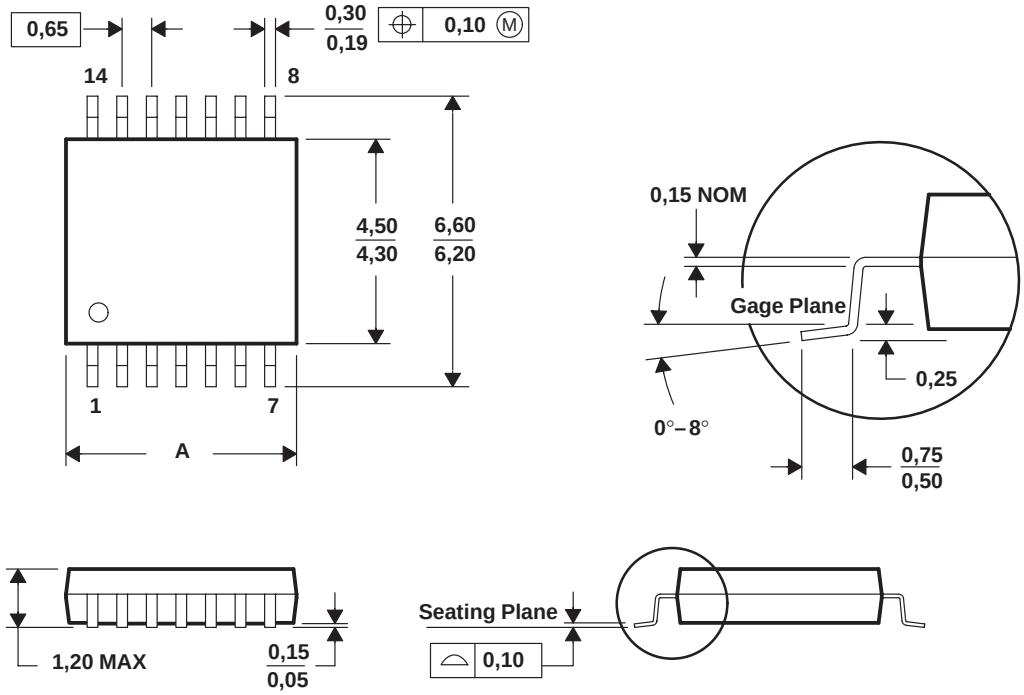


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53126PWR	TSSOP	PW	24	2000	346.0	346.0	33.0
TPS53126RGER	VQFN	RGE	24	3000	346.0	346.0	29.0
TPS53126RGET	VQFN	RGE	24	250	190.5	212.7	31.8

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

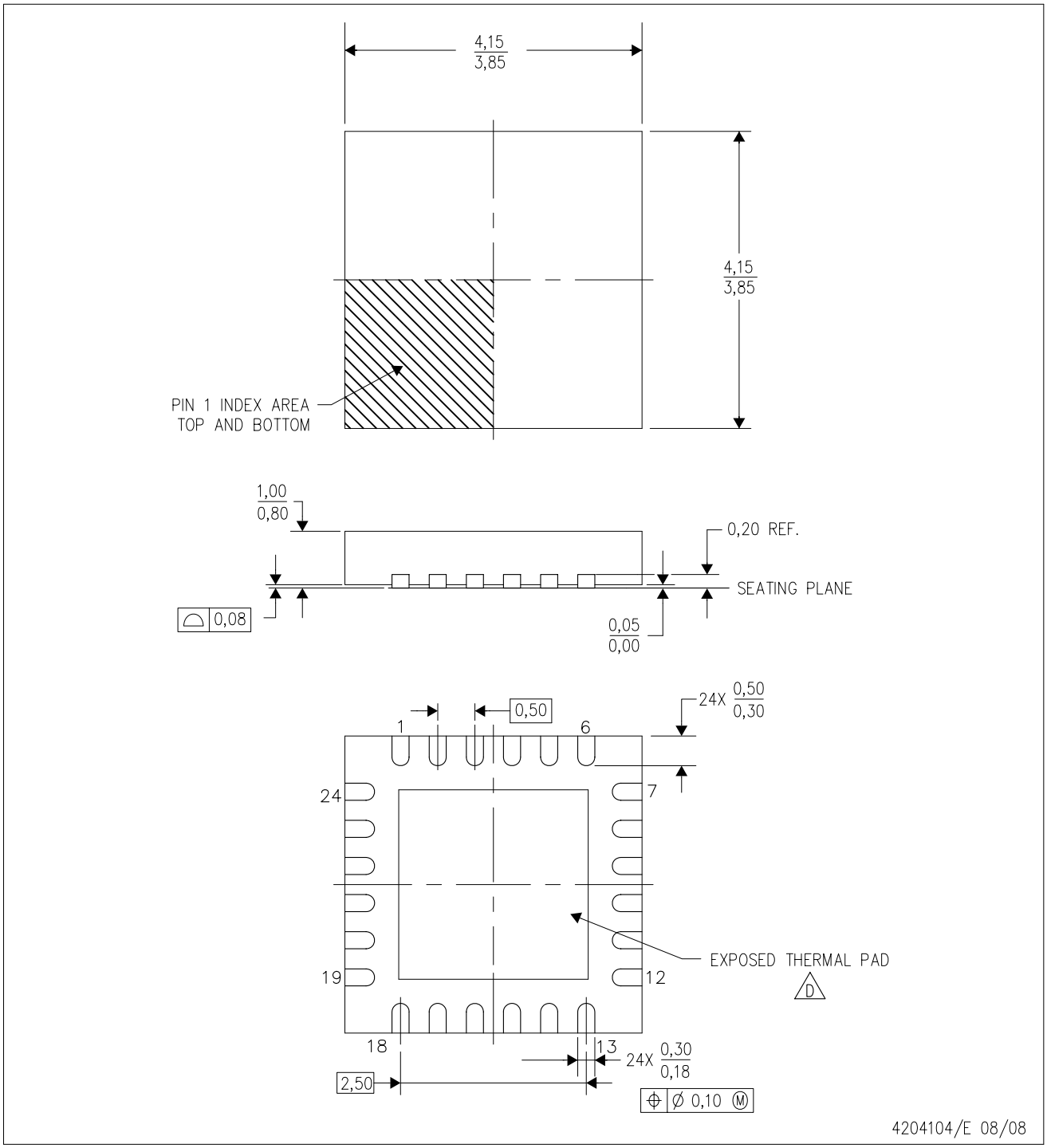


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

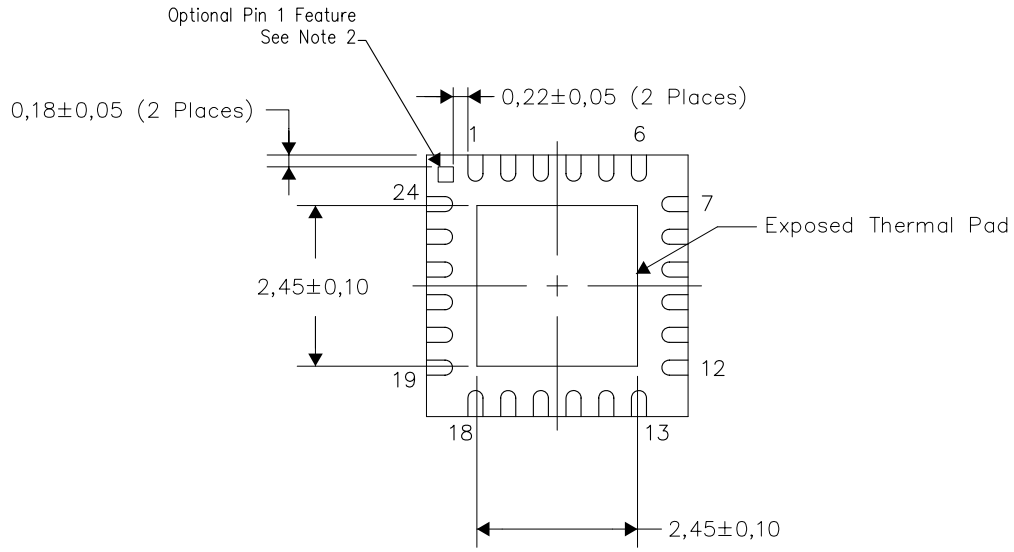
RGE (S–PVQFN–N24)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



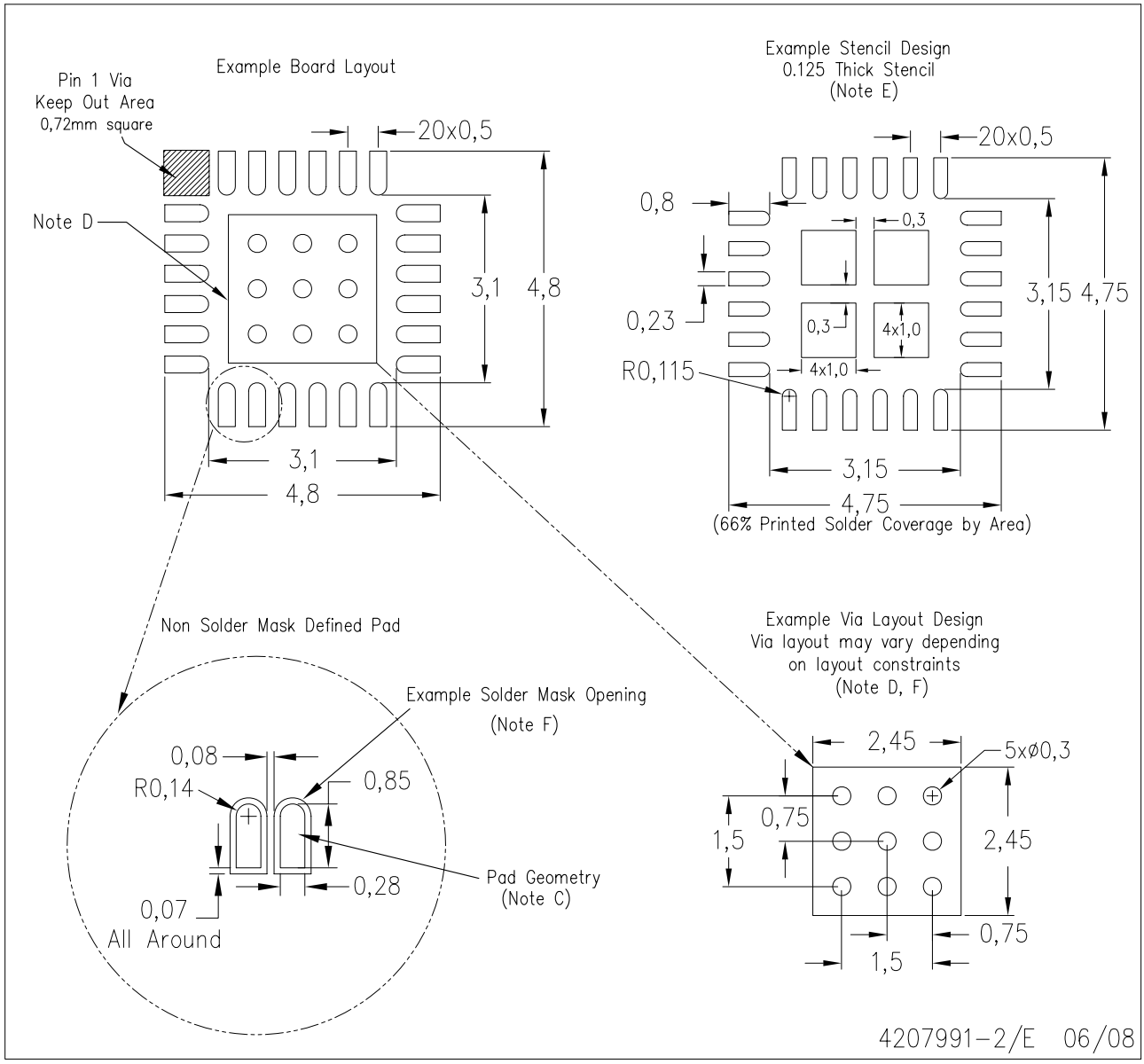
Bottom View

Exposed Thermal Pad Dimensions

NOTES:

1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices
   In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGE (S–PVQFN–N24)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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