



TMUX6104 36-V, Low-Capacitance, Low-Leakage-Current, 4:1 Precision Analog Multiplexer

1 Features

- Low On-Capacitance: 5 pF
- Low Input Leakage: 1 pA
- Low Charge Injection: 0.35 pC
- Rail-to-Rail Operation
- Wide Supply Range: ± 5 V to ± 18 V (Dual Supplies) or 10 V to 36 V (Single Supply)
- Low On-Resistance: 125 Ω
- Transition Time: 88 ns
- Break-Before-Make Switching Action
- EN Pin Connectable to V_{DD} With Integrated Pull-down
- Logic Levels: 2 V to V_{DD}
- Low Supply Current: 17 μ A
- ESD Protection HBM: 2000 V
- Industry-Standard TSSOP Package

2 Applications

- Factory Automation and Industrial Process Controls
- Programmable Logic Controllers (PLC)
- Analog Input Modules
- ATE Test Equipment
- Digital Multimeters
- Battery Monitoring Systems

3 Description

The TMUX6104 is a modern complementary metal-oxide semiconductor (CMOS) analog multiplexer (mux). The TMUX6104 offers 4:1 single-ended switching, and works equally well with either dual supplies (± 5 V to ± 18 V) or a single supply (10 V to 36 V). The device also performs well with symmetric supplies (such as $V_{DD} = 12$ V, $V_{SS} = -12$ V), and unsymmetric supplies (such as $V_{DD} = 12$ V, $V_{SS} = -5$ V). All digital inputs have TTL-logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range.

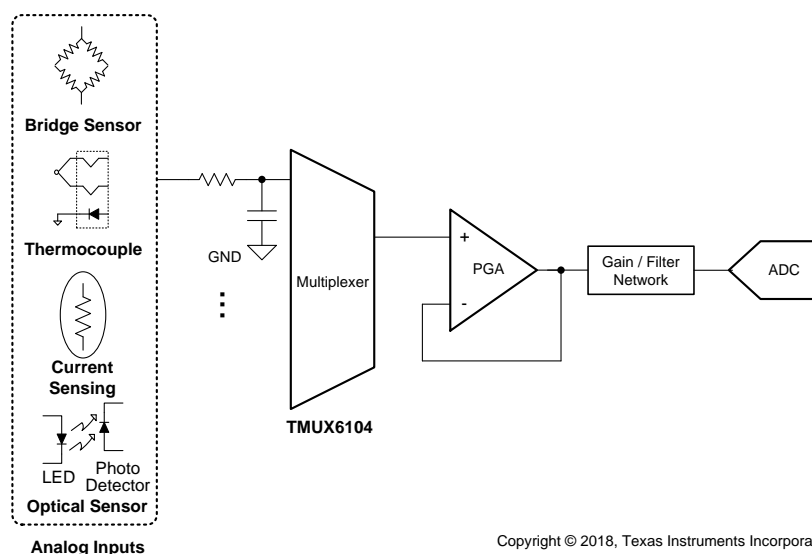
The TMUX6104 has very low on and off leakage currents and ultra-low charge injection, allowing the device to be used in high precision measurement applications. The device also provides excellent isolation capability by blocking signal levels up to the supplies when the switches are in the OFF position. A low supply current of 17 μ A enables usage in portable applications.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX6104	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Schematic



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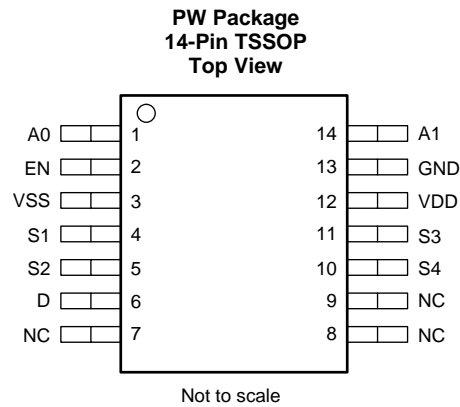
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2018	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	PIN NO.		
A0	1	I	Address line 0
A1	14	I	Address line 1
D	6	I/O	Drain pin. Can be an input or output.
EN	2	I	Active high digital input. When this pin is low, all switches are turned off. When this pin is high, the A0 and A1 logic inputs determine which switch is turned on.
GND	13	P	Ground (0 V) reference
NC	7, 8, 9	No Connect	No internal connection
S1	4	I/O	Source pin 1. Can be an input or output.
S2	5	I/O	Source pin 2. Can be an input or output.
S3	11	I/O	Source pin 3. Can be an input or output.
S4	10	I/O	Source pin 4. Can be an input or output.
V _{DD}	12	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{DD} and GND.
V _{SS}	3	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 μ F to 10 μ F between V _{SS} and GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
$V_{DD}-V_{SS}$	Supply voltage		40	V
V_{DD}		-0.3	40	V
V_{SS}		-40	0.3	V
V_{DIG}	Digital input pin (EN, A0, A1) voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
I_{DIG}	Digital input pin (EN, A0, A1) current	-30	30	mA
V_{ANA_IN}	Analog input pin (Sx) voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
I_{ANA_IN}	Analog input pin (Sx) current	-30	30	mA
V_{ANA_OUT}	Analog output pin (D) voltage	$V_{SS}-0.3$	$V_{DD}+30$	V
I_{ANA_OUT}	Analog output pin (D) current	-30	30	mA
T_A	Ambient temperature	-55	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUX6104	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	64.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{DD_S} ⁽¹⁾	10		36	V
V_{DD_D}	5		18	V
V_{SS} ⁽²⁾	-5		-18	V
$V_{DD} - V_{SS}$	10		36	V

- (1) When $V_{SS} = 0$ V, V_{DD} can range from 10 V to 36 V.
(2) V_{DD} and V_{SS} can be any value as long as $10\text{ V} \leq (V_{DD} - V_{SS}) \leq 36\text{ V}$.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Source pins voltage ⁽³⁾	V_{SS}		V_{DD}	V
V_D	Drain pin voltage	V_{SS}		V_{DD}	V
V_{EN}	Enable pin voltage	V_{SS}		V_{DD}	V
V_A	Address pins voltage	V_{SS}		V_{DD}	V
I_{CH}	Channel current ($T_A = 25^\circ\text{C}$)	-25		25	mA
T_A	Ambient temperature	-40		125	$^\circ\text{C}$

(3) V_S is the voltage on all the S pins.

6.5 Electrical Characteristics (Dual Supplies: $\pm 15\text{ V}$)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15\text{ V}$, and $V_{SS} = -15\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SWITCH						
V _A	Analog signal range	T _A = −40°C to +125°C	V _{SS}		V _{DD}	V
R _{ON}	On-resistance	V _S = 0 V, I _S = 1 mA	125		170	Ω
		V _S = ±10 V, I _S = 1 mA	145		200	Ω
		V _S = ±10 V, I _S = 1 mA, T _A = −40°C to +85°C			230	Ω
		V _S = ±10 V, I _S = 1 mA, T _A = −40°C to +125°C			250	Ω
ΔR _{ON}	On-resistance mismatch between channels	V _S = ±10 V, I _S = 1 mA	2.4		6	Ω
		V _S = ±10 V, I _S = 1 mA, T _A = −40°C to +85°C			9	Ω
		V _S = ±10 V, I _S = 1 mA, T _A = −40°C to +125°C			11	Ω
R _{ON_FLAT}	On-resistance flatness	V _S = −10 V, 0 V, +10 V, I _S = 1 mA	22		45	Ω
		V _S = −10 V, 0 V, +10 V, I _S = 1 mA, T _A = −40°C to +85°C			53	Ω
		V _S = −10 V, 0 V, +10 V, I _S = 1 mA, T _A = −40°C to +125°C			58	Ω
R _{ON_DRIFT}	On-resistance drift	V _S = 0 V		0.52		%/°C
I _{S(OFF)}	Source off leakage current ⁽¹⁾	Switch state is off, V _S = +10 V/ −10 V, V _D = −10 V/ +10 V	−0.04	0.001	0.04	nA
		Switch state is off, V _S = +10 V/ −10 V, V _D = −10 V/ +10 V, T _A = −40°C to +85°C	−0.15		0.15	nA
		Switch state is off, V _S = +10 V/ −10 V, V _D = −10 V/ +10 V, T _A = −40°C to +125°C	TBD		TBD	nA
I _{D(OFF)}	Drain off leakage current ⁽¹⁾	Switch state is off, V _S = +10 V/ −10 V, V _D = −10 V/ +10 V	−0.1	0.005	0.1	nA
		Switch state is off, V _S = +10 V/ −10 V, V _D = −10 V/ +10 V, T _A = −40°C to +85°C	−0.5		0.5	nA
		Switch state is off, V _S = +10 V/ −10 V, V _D = −10 V/ +10 V, T _A = −40°C to +125°C	TBD		TBD	nA

(1) When V_S is positive, V_D is negative, and vice versa.

Electrical Characteristics (Dual Supplies: ± 15 V) (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15$ V, and $V_{SS} = -15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{D(ON)}	Drain on leakage current	Switch state is on, V _S = +10 V/ −10 V, V _D = −10 V/ +10 V	−0.1	0.008	0.1	nA
		Switch state is on, V _S = +10 V/ −10 V, V _D = −10 V/ +10 V, T _A = −40°C to +85°C	−0.5		0.5	nA
		Switch state is on, V _S = +10 V/ −10 V, V _D = −10 V/ +10 V, T _A = −40°C to +125°C	TBD		TBD	nA
DIGITAL INPUT (EN, Ax pins)						
V _{IH}	Logic voltage high		2			V
V _{IL}	Logic voltage low				0.8	V
R _{PD(EN)}	Pull-down resistance on EN pin			6		MΩ
POWER SUPPLY						
I _{DD}	V _{DD} supply current	V _A = 0 V or 3.3 V, V _S = 0 V , V _{EN} = 3.3 V		17	24	μA
		V _A = 0 V or 3.3 V, V _S = 0 V , V _{EN} = 3.3 V, T _A = −40°C to +85°C			25	μA
		V _A = 0 V or 3.3 V, V _S = 0 V , V _{EN} = 3.3 V, T _A = −40°C to +125°C			27	μA
I _{SS}	V _{SS} supply current	V _A = 0 V or 3.3 V, V _S = 0 V , V _{EN} = 3.3 V		7	12	μA
		V _A = 0 V or 3.3 V, V _S = 0 V , V _{EN} = 3.3 V, T _A = −40°C to +85°C			13	μA
		V _A = 0 V or 3.3 V, V _S = 0 V , V _{EN} = 3.3 V, T _A = −40°C to +125°C			15	μA

6.6 Switching Characteristics (Dual Supplies: ± 15 V)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15$ V, and $V_{SS} = -15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	$V_S = \pm 10$ V, $R_L = 300$ Ω , $C_L = 35$ pF		85	TBD	ns
		$V_S = \pm 10$ V, $R_L = 300$ Ω , $C_L = 35$ pF, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			TBD	ns
		$V_S = \pm 10$ V, $R_L = 300$ Ω , $C_L = 35$ pF, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			TBD	ns
t_{OFF}	Enable turn-off time	$V_S = \pm 10$ V, $R_L = 300$ Ω , $C_L = 35$ pF		53	TBD	ns
		$V_S = \pm 10$ V, $R_L = 300$ Ω , $C_L = 35$ pF, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			TBD	ns
		$V_S = \pm 10$ V, $R_L = 300$ Ω , $C_L = 35$ pF, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			TBD	ns
t_{TRAN}	Transition time	$V_S = 10$ V, $R_L = 300$ Ω , $C_L = 35$ pF		88	TBD	ns
		$V_S = 10$ V, $R_L = 300$ Ω , $C_L = 35$ pF, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			TBD	ns
		$V_S = 10$ V, $R_L = 300$ Ω , $C_L = 35$ pF, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			TBD	ns
t_{BBM}	Break-before-make time delay	$V_S = 10$ V, $R_L = 300$ Ω , $C_L = 35$ pF, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	30	50		ns
Q_I	Charge injection	$V_S = 0$ V, $R_S = 0$ Ω , $C_L = 1$ nF		-0.35		pC
		$V_S = -15$ V to 15 V, $R_S = 0$ Ω , $C_L = 1$ nF		-0.41		pC
O_{ISO}	Off-isolation	$R_L = 50$ Ω , $C_L = 5$ pF, $f = 1$ MHz		-86		dB
X_{TALK}	Channel-to-channel crosstalk	$R_L = 50$ Ω , $C_L = 5$ pF, $f = 1$ MHz, nonadjacent channels		-105		dB
		$R_L = 50$ Ω , $C_L = 5$ pF, $f = 1$ MHz, adjacent channels		-87		dB
BW	-3dB Bandwidth	$R_L = 50$ Ω , $C_L = 5$ pF		400		MHz

Switching Characteristics (Dual Supplies: ± 15 V) (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 15$ V, and $V_{SS} = -15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion + noise $R_L = 10\text{k}\Omega$, $C_L = 5\text{ pF}$, $f = 20\text{ Hz}$ to 20 kHz		0.15		%
C_{IN}	Digital input capacitance $V_{IN} = 0$ V or V_{DD}		1.2		pF
$C_{S(OFF)}$	Source off-capacitance $V_S = 0$ V, $f = 1$ MHz		1.6	TBD	pF
$C_{D(OFF)}$	Drain off-capacitance $V_S = 0$ V, $f = 1$ MHz		3.8	TBD	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance $V_S = 0$ V, $f = 1$ MHz		5.0	TBD	pF

6.7 Electrical Characteristics (Single Supply: 12 V)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 12$ V, and $V_{SS} = 0$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SWITCH					
V_A	Analog signal range $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	V_{SS}		V_{DD}	V
R_{ON}	On-resistance $V_S = 10$ V, $I_S = 1$ mA		235	345	Ω
	$V_S = 10$ V, $I_S = 1$ mA, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			400	Ω
	$V_S = 10$ V, $I_S = 1$ mA, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			440	Ω
ΔR_{ON}	On-resistance mismatch between channels $V_S = 10$ V, $I_S = 1$ mA		4	12	Ω
	$V_S = 10$ V, $I_S = 1$ mA, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			19	Ω
	$V_S = 10$ V, $I_S = 1$ mA, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			23	Ω
R_{ON_DRIFT}	On-resistance drift $V_S = 0$ V		0.47		%/ $^\circ\text{C}$
$I_{S(OFF)}$	Source off leakage current ⁽¹⁾ Switch state is off, $V_S = 10$ V/ 1 V, $V_D = 1$ V/ 10 V	-0.04	0.001	0.04	nA
	Switch state is off, $V_S = 10$ V/ 1 V, $V_D = 1$ V/ 10 V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-0.15		0.15	nA
	Switch state is off, $V_S = 10$ V/ 1 V, $V_D = 1$ V/ 10 V, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	TBD		TBD	nA
$I_{D(OFF)}$	Drain off leakage current ⁽¹⁾ Switch state is off, $V_S = 10$ V/ 1 V, $V_D = 1$ V/ 10 V	-0.1	0.005	0.1	nA
	Switch state is off, $V_S = 10$ V/ 1 V, $V_D = 1$ V/ 10 V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-0.5		0.5	nA
	Switch state is off, $V_S = 10$ V/ 1 V, $V_D = 1$ V/ 10 V, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	TBD		TBD	nA
$I_{D(ON)}$	Drain on leakage current Switch state is on, $V_S =$ floating, $V_D = 1$ V/ 10 V	-0.1	0.008	0.1	nA
	Switch state is on, $V_S =$ floating, $V_D = 1$ V/ 10 V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	-0.5		0.5	nA
	Switch state is on, $V_S =$ floating, $V_D = 1$ V/ 10 V, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	TBD		TBD	nA
DIGITAL INPUT (EN, Ax pins)					
V_{IH}	Logic voltage high	2			V
V_{IL}	Logic voltage low			0.8	V
$R_{PD(EN)}$	Pull-down resistance on EN pin		6		M Ω
POWER SUPPLY					

(1) When V_S is positive, V_D is negative, and vice versa.

Electrical Characteristics (Single Supply: 12 V) (continued)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, and $V_{SS} = 0\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD} V_{DD} supply current	$V_A = 0\text{ V}$ or 3.3 V , $V_S = 0\text{ V}$, $V_{EN} = 3.3\text{ V}$		12	18	μA
	$V_A = 0\text{ V}$ or 3.3 V , $V_S = 0\text{ V}$, $V_{EN} = 3.3\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			19	μA
	$V_A = 0\text{ V}$ or 3.3 V , $V_S = 0\text{ V}$, $V_{EN} = 3.3\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			21	μA

6.8 Switching Characteristics (Single Supply: 12 V)

at $T_A = 25^\circ\text{C}$, $V_{DD} = 12\text{ V}$, and $V_{SS} = 0\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON} Enable turn-on time	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$		91	TBD	ns
	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			TBD	ns
	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			TBD	ns
t_{OFF} Enable turn-off time	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$		52	TBD	ns
	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			TBD	ns
	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			TBD	ns
t_{TRAN} Transition time	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$		94	TBD	ns
	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			TBD	ns
	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			TBD	ns
t_{BBM} Break-before-make time delay	$V_S = 8\text{ V}$, $R_L = 300\ \Omega$, $C_L = 35\text{ pF}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	30	55		ns
Q_J Charge injection	$V_S = 6\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$		-0.15		pC
	$V_S = 0\text{ V}$ to 12 V , $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$		-0.15		pC
O_{ISO} Off-isolation	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$		-86		dB
X_{TALK} Channel-to-channel crosstalk	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, nonadjacent channels		-107		dB
	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, adjacent channels		-87		dB
BW -3dB Bandwidth	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$		300		MHz
C_{IN} Digital input capacitance	$V_{IN} = 0\text{ V}$ or V_{DD}		1.0		pF
$C_{S(OFF)}$ Source off-capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$		1.9	TBD	pF
$C_{D(OFF)}$ Drain off-capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$		4.6	TBD	pF
$C_{S(ON)}$, $C_{D(ON)}$ Source and drain on-capacitance	$V_S = 6\text{ V}$, $f = 1\text{ MHz}$		6.3	TBD	pF

7 Detailed Description

7.1 Overview

7.1.1 On-Resistance

The on-resistance of the TMUX6104 is the ohmic resistance across the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 1. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in Equation 1:

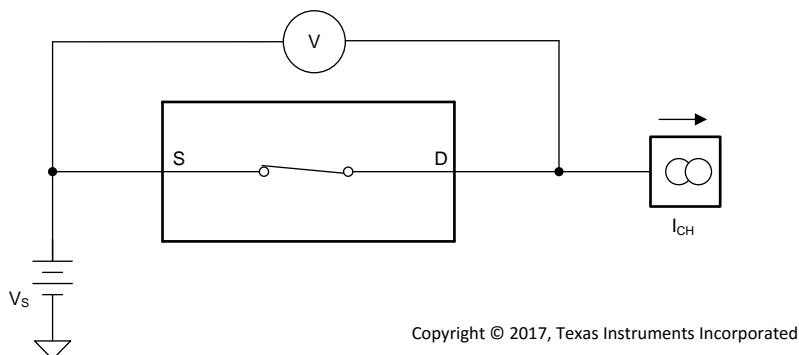


Figure 1. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \quad (1)$$

7.1.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in Figure 2

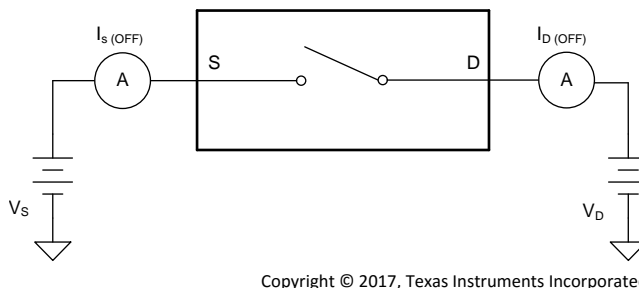
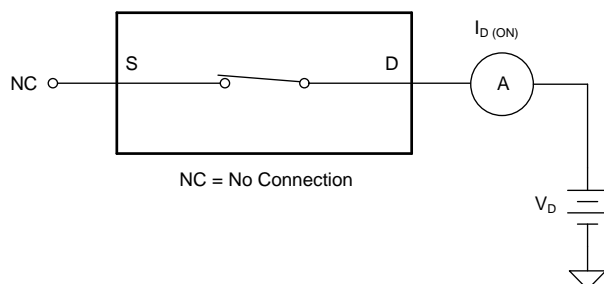


Figure 2. Off-Leakage Measurement Setup

Overview (continued)

7.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. Figure 3 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.



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Figure 3. On-Leakage Measurement Setup

7.1.4 Transition Time

Transition time is defined as the time taken by the output of the TMUX6104 to rise or fall to 90% of the transition after the digital address signal has fallen or risen to 50% of the transition. Figure 4 shows the setup used to measure transition time, denoted by the symbol t_{TRAN} .

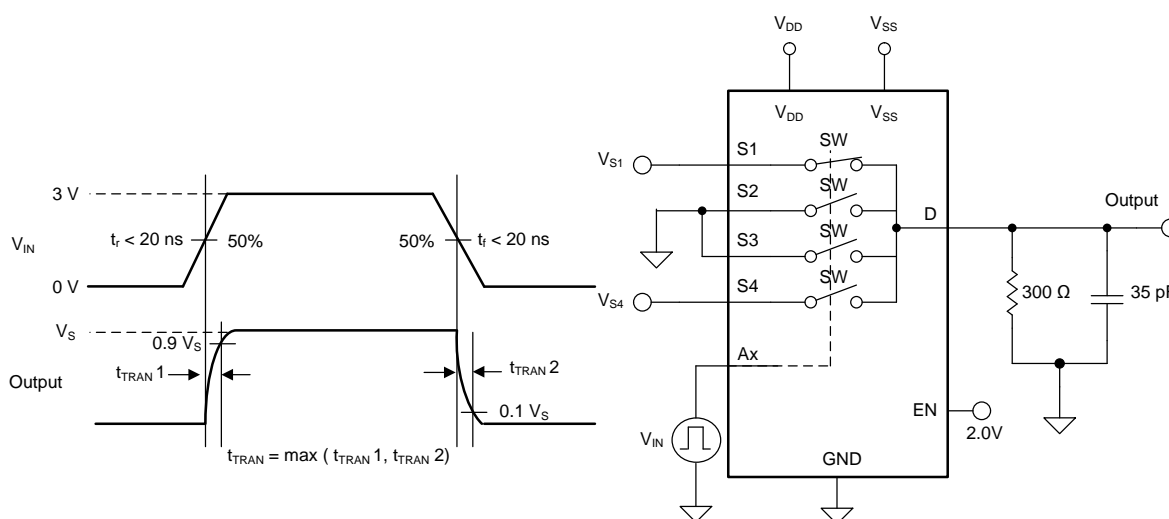


Figure 4. Transition-Time Measurement Setup

Overview (continued)

7.1.5 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the TMUX6104 is switching. The TMUX6104 output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 5 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM} .

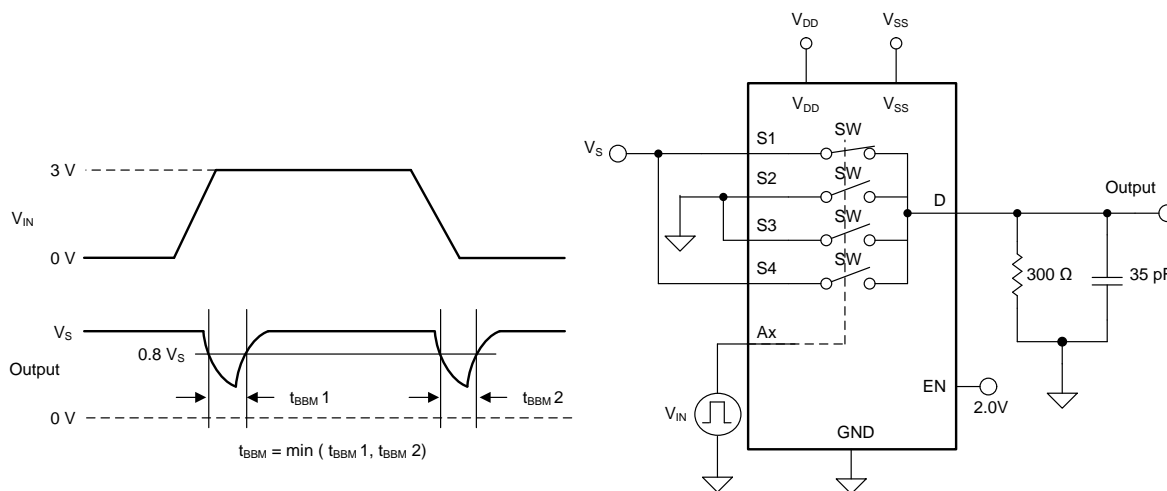


Figure 5. Break-Before-Make Delay Measurement Setup

7.1.6 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the TMUX6104 to rise to a 90% final value after the enable signal has risen to a 50% final value. Figure 6 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol $t_{ON}(EN)$.

Turn off time is defined as the time taken by the output of the TMUX6104 to fall to a 10% initial value after the enable signal has fallen to a 50% initial value. Figure 6 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol $t_{OFF}(EN)$.

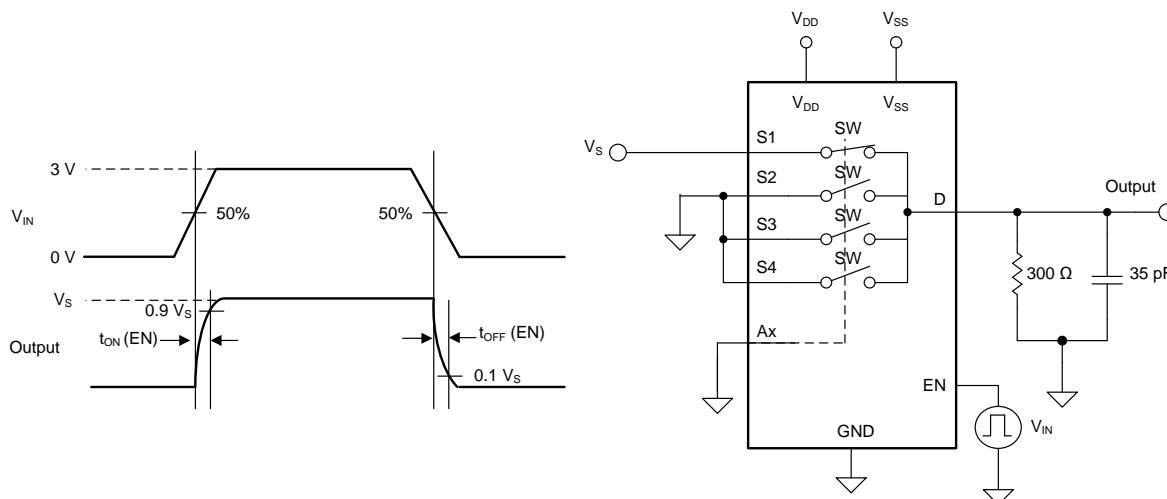


Figure 6. Turn-On and Turn-Off Time Measurement Setup

Overview (continued)

7.1.7 Charge Injection

The TMUX6104 have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ} . Figure 7 shows the setup used to measure charge injection from source (Sx) to drain (D).

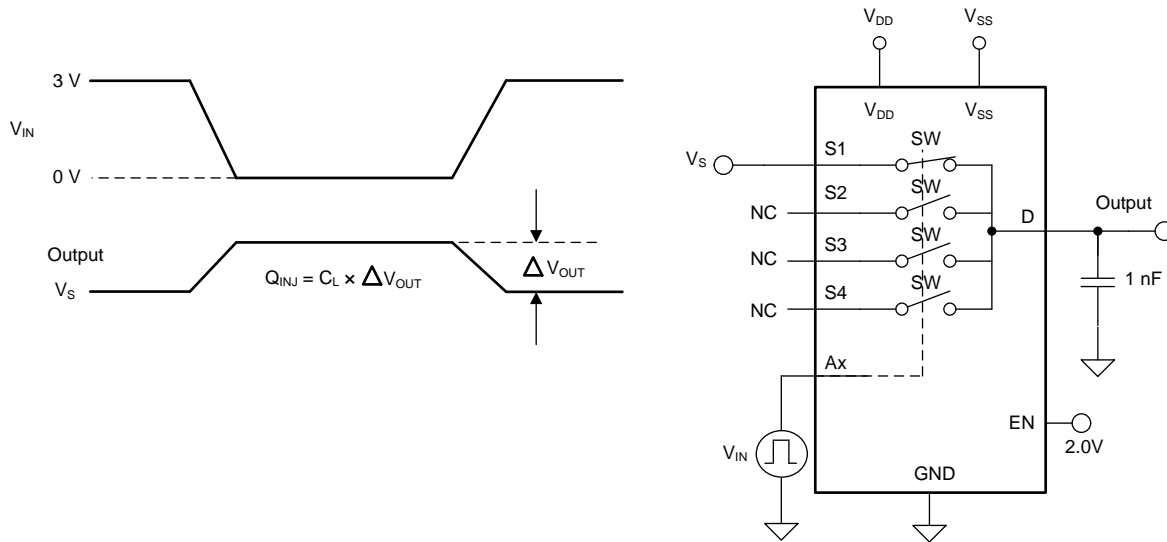


Figure 7. Charge-Injection Measurement Setup

7.1.8 Off Isolation

Off isolation is defined as the voltage at the drain pin (D) of the TMUX6104 when a 1-V_{RMS} signal is applied to the source pin (Sx) of an off-channel. Figure 8 shows the setup used to measure off isolation. Use Equation 2 to compute off isolation.

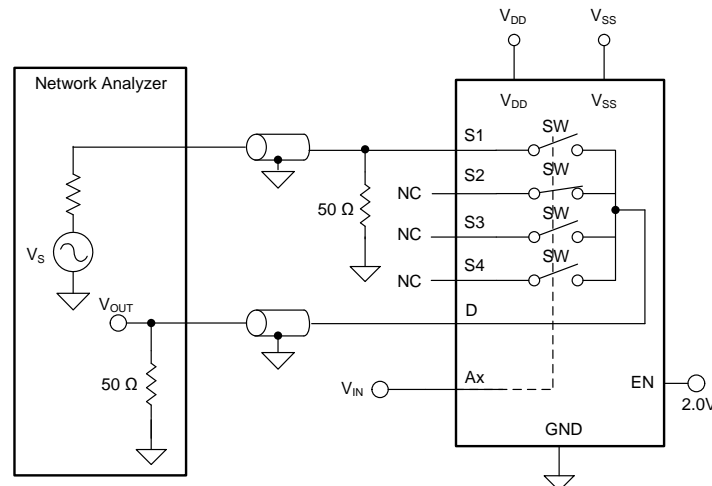


Figure 8. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log} \left(\frac{V_{OUT}}{V_S} \right)$$

(2)

Overview (continued)

7.1.9 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx) of an off-channel, when a $1\text{-}V_{\text{RMS}}$ signal is applied at the source pin (Sx) of an on-channel. Figure 9 shows the setup used to measure, and Equation 3 is the equation used to compute, channel-to-channel crosstalk.

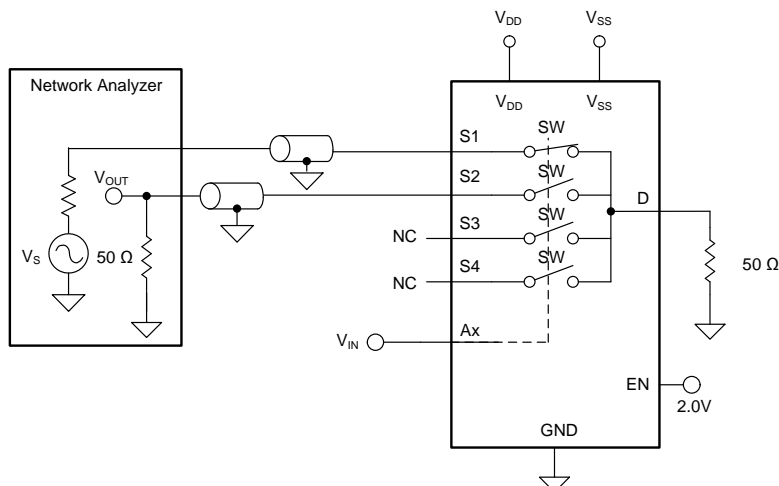


Figure 9. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log} \left(\frac{V_{\text{OUT}}}{V_{\text{S}}} \right) \quad (3)$$

7.1.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by $< 3 \text{ dB}$ when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the TMUX6104. Figure 10 shows the setup used to measure bandwidth of the mux. Use Equation 4 to compute the attenuation.

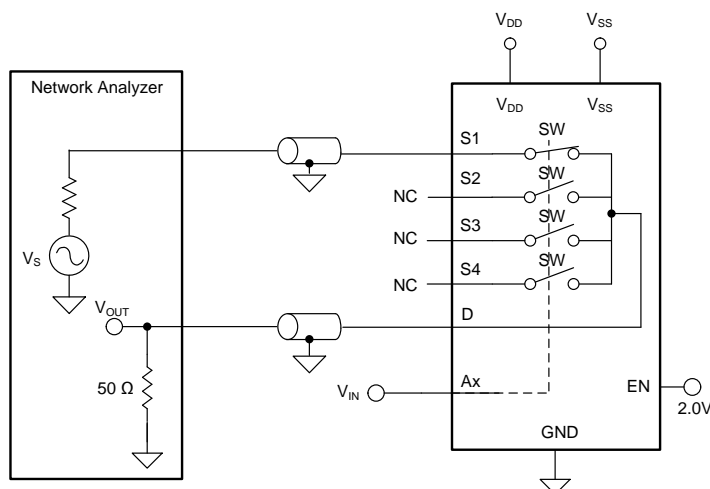


Figure 10. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log} \left(\frac{V_2}{V_1} \right) \quad (4)$$

Overview (continued)

7.1.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX6104 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N.

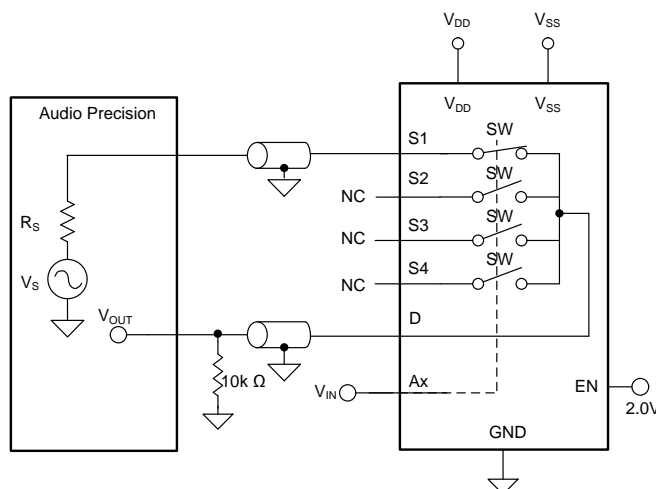


Figure 11. THD+N Measurement Setup

7.1.12 AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

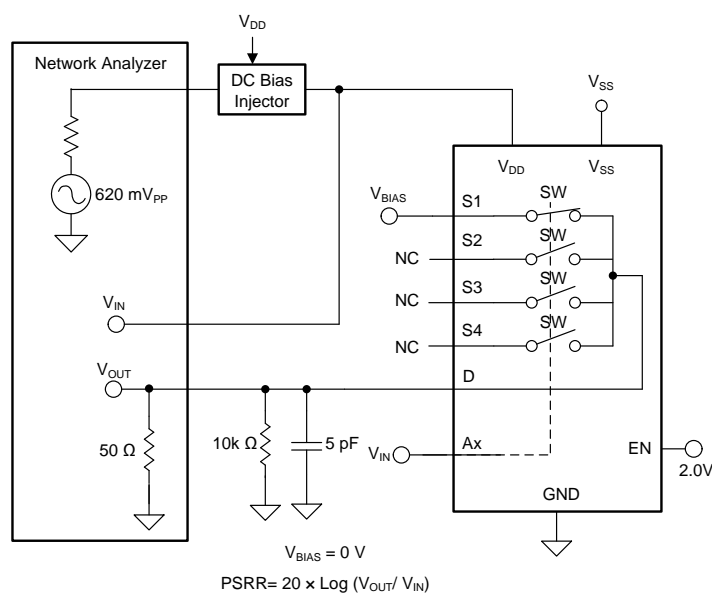
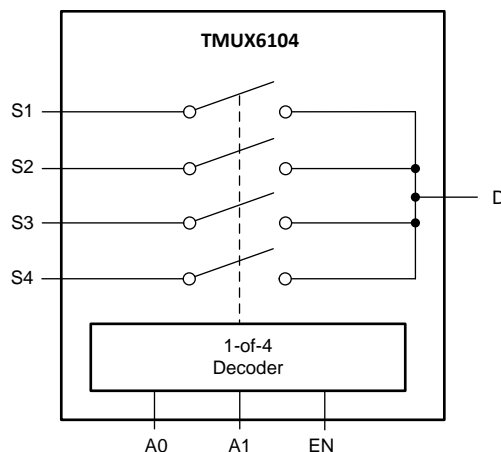


Figure 12. AC PSRR Measurement Setup

Overview (continued)

The [Functional Block Diagram](#) section provides a top-level block diagram of the TMUX6104. The TMUX6104 is a 4-channel, single-ended, analog multiplexer. Each channel is turned on or turned off based on the state of the address lines and enable pin.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Ultralow Leakage Current

The TMUX6104 provide extremely low on- and off-leakage currents. The TMUX6104 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. [Figure 13](#) shows typical leakage currents of the TMUX6104 versus temperature.

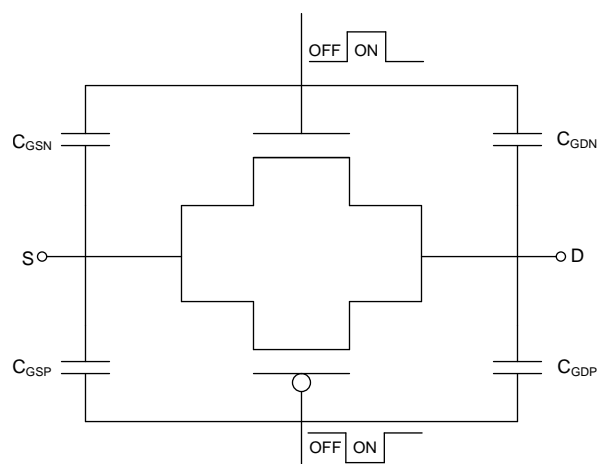


Figure 13. Leakage Current vs Temperature

7.3.2 Ultralow Charge Injection

The TMUX6104 is implemented with simple transmission gate topology, as shown in [Figure 14](#). Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

Feature Description (continued)



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Figure 14. Transmission Gate Topology

The TMUX6119 utilizes special charge-injection cancellation circuitry that reduces the source (Sx) to drain (D) charge injection to as low as -0.35 pC at $V_S = 0$ V, and ± 0.41 pC in the full signal range, as shown in [Figure 15](#).



Figure 15. Source-to-Drain Charge Injection vs Source or Drain Voltage

The drain (D)-to-source (Sx) charge injection becomes important when the device is used as a demultiplexer (demux), where the drain (D) becomes the input and the source (Sx) becomes the output. [Figure 16](#) shows the drain-to-source charge injection across the full signal range.



Figure 16. Drain-to-Source Charge Injection vs Source or Drain Voltage

Feature Description (continued)

7.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX6104 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each TMUX6104 channel has very similar characteristics in both directions. The valid analog signal for TMUX6104 ranges from V_{SS} to V_{DD} . The input signal to the TMUX6104 swings from V_{SS} to V_{DD} without any significant degradation in performance.

7.4 Device Functional Modes

When the EN pin of the TMUX6104 is pulled high, one of the four switches is closed based on the state of the address pins (A0 and A1). When the EN pin is pulled low, all four switches remain open irrespective of the state of the address pins. The EN pin is weakly pull-down internally through a 6 M Ω resistor; thereby, setting each channel to the open state if the EN pin is not actively driven. The address pins are also weakly pulled-down through an internal 6 M Ω resistor, allowing channel 1 (S1 to D) to be selected by default when EN pin is driven high. Both the EN pin and the address pins can be connected to V_{DD} (as high as 36 V).

7.4.1 Truth Table

Table 1. TMUX6104 Truth Table

EN	A1	A0	STATE
0	X ⁽¹⁾	X ⁽¹⁾	All channels are off
1	0	0	Channel 1
1	0	1	Channel 2
1	1	0	Channel 3
1	1	1	Channel 4

(1) X denotes *don't care*..

8 Application and Implementation

NOTE

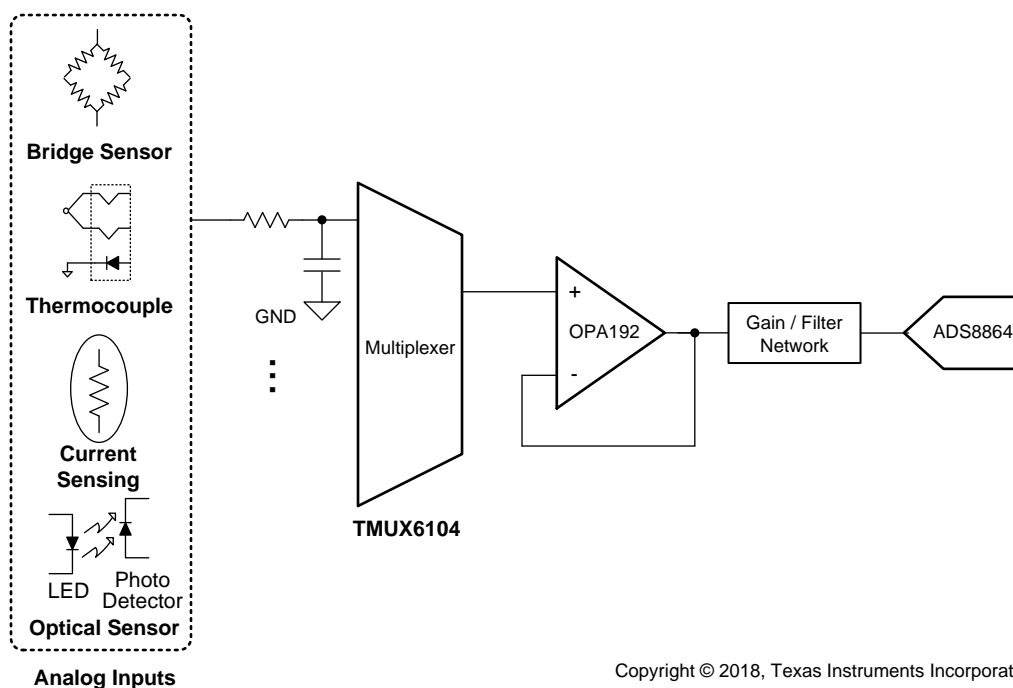
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMUX6104 offers outstanding input/output leakage currents and ultralow charge injection. These devices operate up to 36 V, and offer true rail-to-rail input and output. The on-capacitance of the TMUX6104 is very low. These features makes the TMUX6104 a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

8.2 Typical Application

Figure 17 shows a 16-bit, differential, 4-channel, multiplexed, data-acquisition system. This example is typical in industrial applications that require low distortion and a high-voltage input. The circuit uses the [ADS8864](#), a 16-bit, 400-kSPS successive-approximation-resistor (SAR) analog-to-digital converter (ADC), along with a precision, high-voltage, signal-conditioning front end, and a 4-channel single-ended mux. This TI Precision Design details the process for optimizing the precision, high-voltage, front-end drive circuit using the TMUX6104 and [OPA192](#) to achieve excellent dynamic performance and linearity with the ADS8864.



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Figure 17. 16-Bit Precision Multiplexed Data-Acquisition System for High-Voltage Inputs With Lowest Distortion

Typical Application (continued)

8.2.1 Design Requirements

The primary objective is to design a ± 15 V, single-ended, 4-channel, multiplexed, data-acquisition system with lowest distortion using the 16-bit ADS8864 at a throughput of 400 kSPS for a 10-kHz, full-scale, pure, sine-wave input. The design requirements for this block design are:

- System supply voltage: ± 15 V
- ADC supply voltage: 3.3 V
- ADC sampling rate: 400 kSPS
- ADC reference voltage (REFP): 4.096 V
- System input signal: A high-voltage differential input signal with a peak amplitude of 15 V and frequency (f_{IN}) of 10 kHz are applied to each differential input of the mux.

8.2.2 Detailed Design Procedure

The purpose of this precision design is to design an optimal, high-voltage, multiplexed, data-acquisition system for highest system linearity and fast settling. The overall system block diagram is illustrated in [Figure 17](#). The circuit is a multichannel, data-acquisition signal chain consisting of an input low-pass filter, mux, mux output buffer, and attenuating SAR ADC driver. The architecture allows fast sampling of multiple channels using a single ADC, providing a low-cost solution. This design systematically approaches each analog circuit block to achieve a 16-bit settling for a full-scale input stage voltage and linearity for a 10-kHz sinusoidal input signal at each input channel.

8.2.3 Application Curve

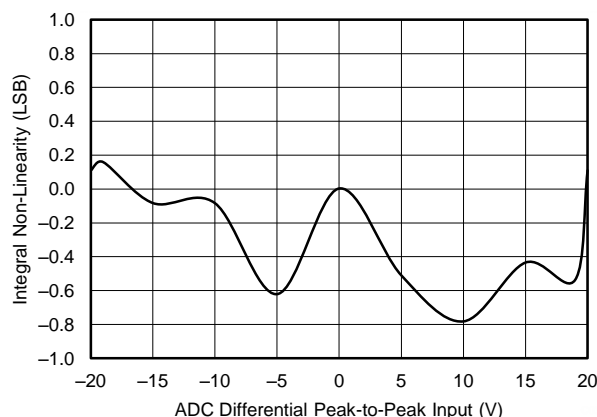


Figure 18. ADC 16-Bit Linearity Error for the Multiplexed Data-Acquisition Block

9 Power Supply Recommendations

The TMUX6104 operates across a wide supply range of ± 5 V to ± 18 V (10 V to 36 V in single-supply mode). The device also perform well with unsymmetric supplies such as $V_{DD} = 12$ V and $V_{SS} = -5$ V. For reliable operation, use a supply decoupling capacitor ranging between 0.1 μ F to 10 μ F at both the V_{DD} and V_{SS} pins to ground.

The on-resistance of the TMUX6104 varies with supply voltage, as illustrated in [Figure 19](#)



Figure 19. On-Resistance Variation With Supply and Input Voltage

10 Layout

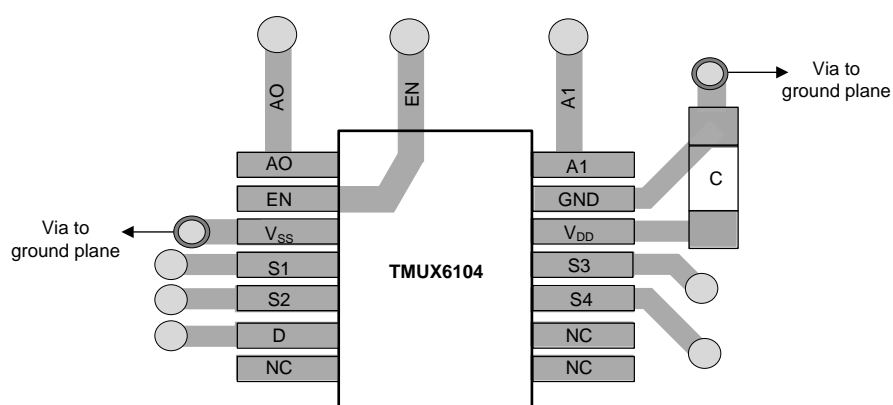
10.1 Layout Guidelines

Figure 20 illustrates an example of a PCB layout with the TMUX6104.

Some key considerations are:

1. Decouple the V_{DD} and V_{SS} pins with a 0.1- μ F capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
2. Keep the input lines as short as possible.
3. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
4. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

10.2 Layout Example



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Figure 20. TMUX6104 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- [ADS8664 12-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges \(SBAS492\)](#)
- [OPA192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-Trim™ \(SBOS620\)](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUX6104PWR	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125	PMX6104	Samples
TMUX6104PWR	PREVIEW	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

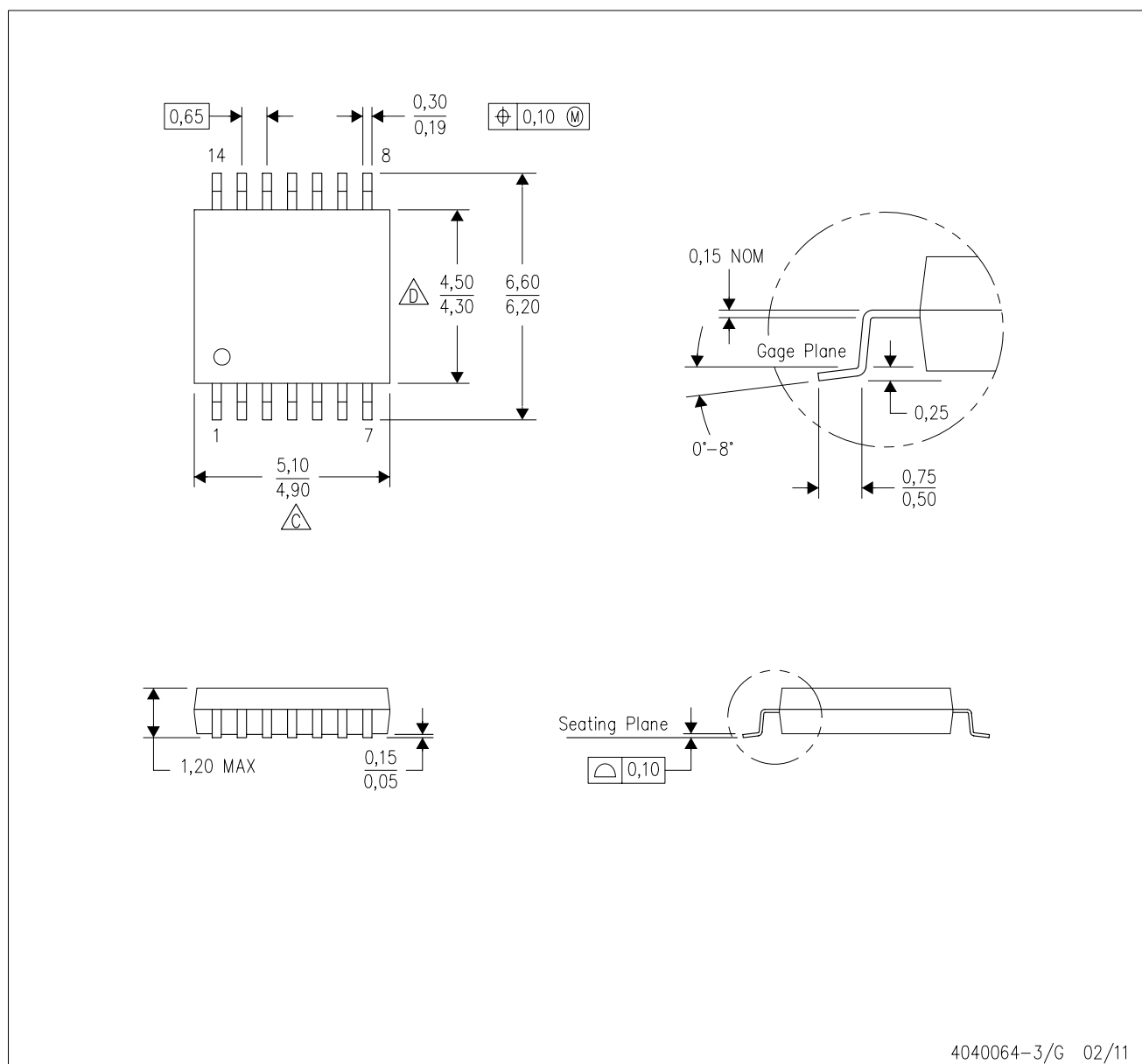
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PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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