

1-A Dual-HBD (Dual-Half-Bridge Driver)

TLE 4207

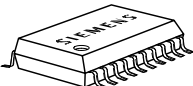
Overview

Features

- Delivers up to 0.8 A continuous
- Optimized for DC motor management applications
- Very low current consumption in stand-by (Inhibit) mode
- Low saturation voltage; typ.1.2 V total @ 25 °C; 0.4 A
- Output protected against short circuit
- Error flag diagnosis
- Overvoltage lockout and diagnosis
- Undervoltage lockout
- CMOS/TTL compatible inputs with hysteresis
- No crossover current
- Internal clamp diodes
- Overtemperature protection with hysteresis and diagnosis
- Enhanced power P-DSO-Package



P-DSO-14-4



P-DSO-20-6

Type	Ordering Code	Package
TLE 4207 G	Q67006-A9275	P-DSO-14-4
TLE 4207 GL	on request	P-DSO-20-6

Description

The TLE 4207 is a fully protected **Dual-Half-Bridge-Driver** designed specially for automotive and industrial motion control applications.

The part is built using the Siemens bipolar high voltage power technology DOPL.

The actuator (DC motor) can be connected direct between the halfbridges. Operation modes forward (cw), reverse (ccw), brake and high impedance are invoked from a standard interface. The standard enhanced power P-DSO-14 package meets the application requirements and saves PCB-board space and costs.

Furthermore the built in features like diagnosis, over- and undervoltage-lockout, short-circuit-protection, over-temperature-protection and the very low quiescent current in stand-by mode will open a wide range of automotive and industrial applications.

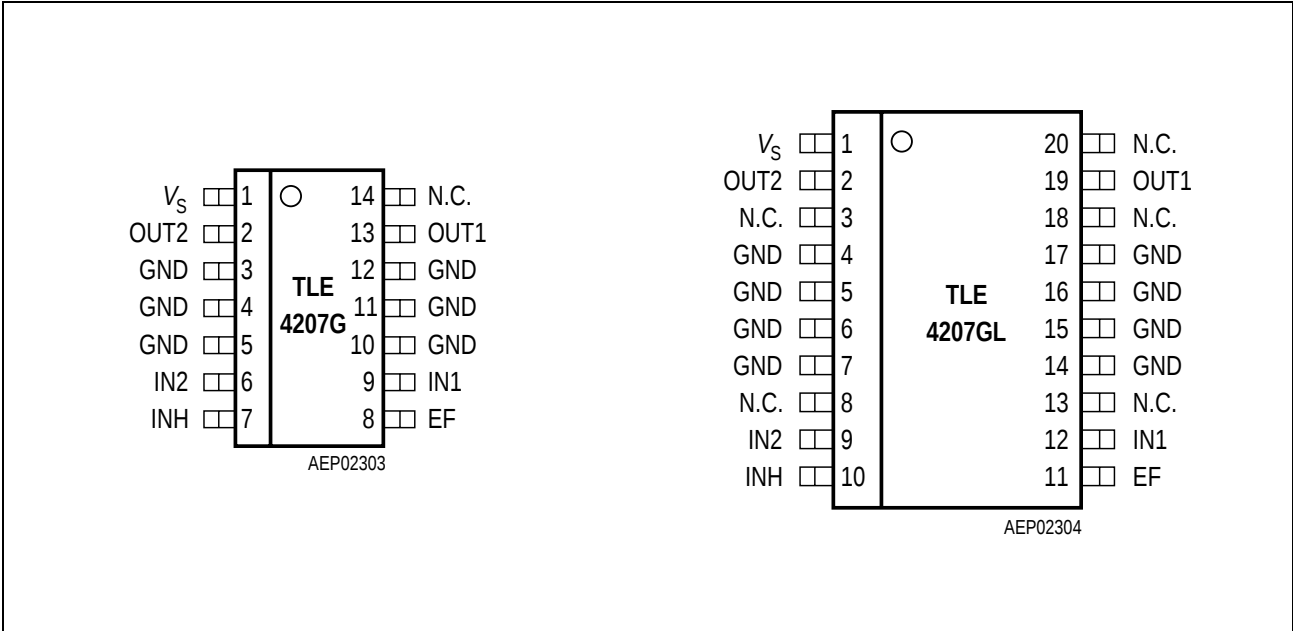


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

Pin No. P-DSO-14-4	Pin No. P-DSO-20-6	Symbol	Function
1	1	V_S	Power supply voltage; positive reference potential for blocking capacitor
2	2	OUT2	Power-output 2; full short circuit protected; with integrated clamp diodes
3, 4, 5, 10, 11, 12	4, 5, 6, 7, 14, 15, 16, 17	GND	Ground; negative reference potential for blocking capacitor
6	9	IN2	Input channel 2; controls OUT2 (not inverted)
7	10	INH	Inhibit input; low = IC in stand-by
8	11	EF	Error Flag output; open collector; low = error
9	12	IN1	Input channel 1; controls OUT1 (not inverted)
13	19	OUT1	Power output 1; full short circuit protected; with integrated clamp diodes
14	3, 8, 13, 18, 20	N.C.	Not connected

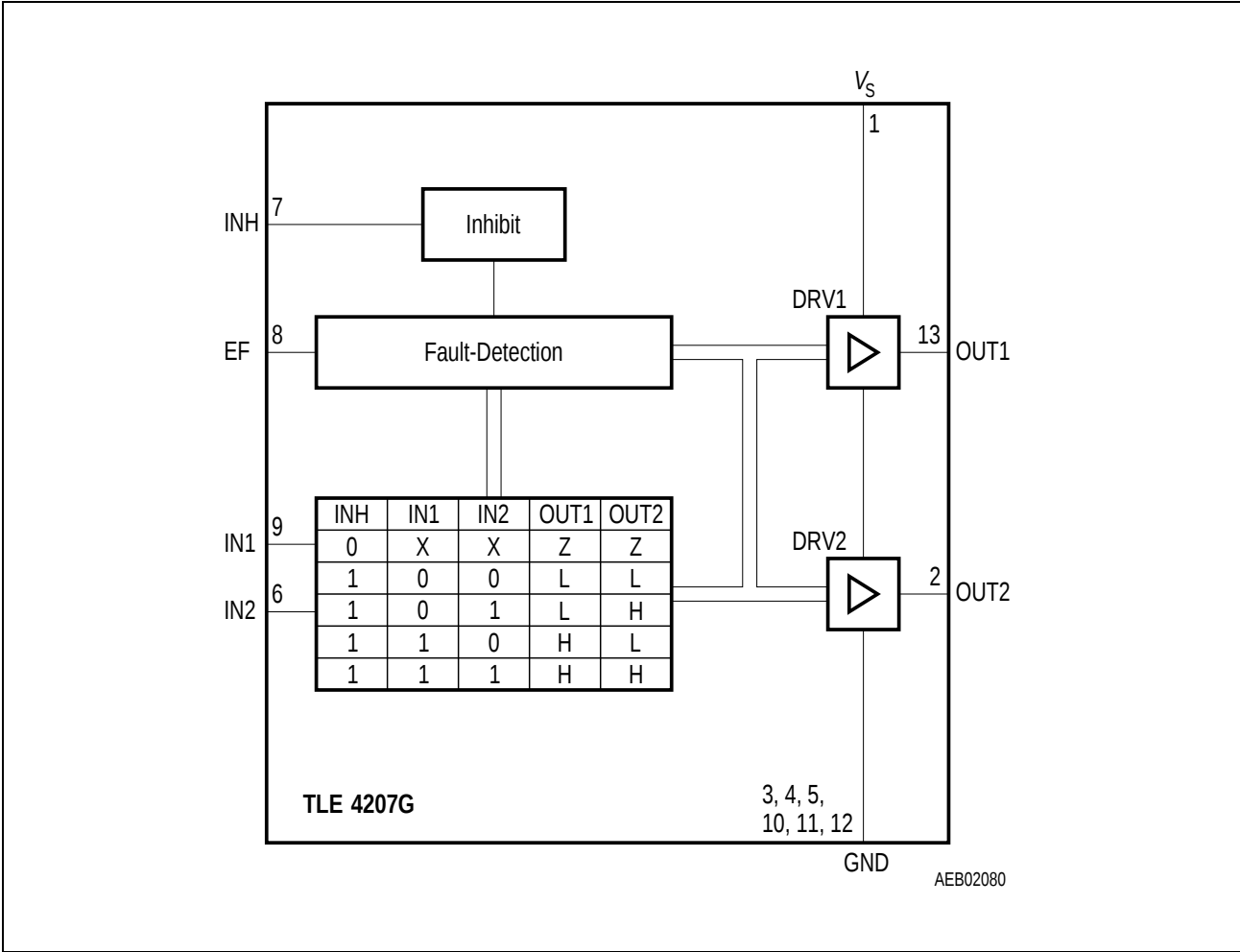


Figure 2 Block Diagram

Functional Truth Table

INH	IN1	IN2	OUT1	OUT2	Mode
0	X	X	Z	Z	Stand-By
1	0	0	L	L	Brake LL
1	0	1	L	H	CW
1	1	0	H	L	CCW
1	1	1	H	H	Brake HH

IN:

0 = Logic LOW
1 = Logic HIGH
X = don't care

OUT:

Z = Output in tristate condition
L = Output in sink condition
H = Output in source condition

Diagnosis

EF	Error
1	no error
0	over temperature
0	over voltage

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

Voltages

Supply voltage	V_S	- 0.3	45	V	–
Supply voltage	V_S	- 1	–	V	$t < 0.5 \text{ s}; I_S > - 2 \text{ A}$
Logic input voltages (IN1; IN2; INH)	V_I	- 5	20	V	$0 \text{ V} < V_S < 45 \text{ V}$
Logic output voltage (EF)	V_{EF}	- 0.3	20	V	$0 \text{ V} < V_S < 45 \text{ V}$

Currents

Output current (cont.)	I_{OUT1-2}	–	–	A	internally limited
Output current (peak)	I_{OUT1-2}	–	–	A	internally limited
Output current (diode)	I_{OUT1-2}	- 1	1	A	–
Output current (EF)	I_{OUT1-2}	- 2	5	mA	–

Temperatures

Junction temperature	T_j	- 40	150	°C	–
Storage temperature	T_{stg}	- 50	150	°C	–

Thermal Resistances

Junction pin	$R_{thj-pin}$	–	25	K/W	measured to pin 5
Junction ambient	R_{thjA}	–	65	K/W	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	$V_{UV\ OFF}$	18	V	After V_S rising above $V_{UV\ ON}$
Supply voltage increasing	V_S	- 0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	V_S	- 0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Logic input voltage (IN1; IN2; INH)	V_I	- 2	18	V	-
Junction temperature	T_j	- 40	150	°C	-

Note: In the operating range the functions given in the circuit description are fulfilled.

Electrical Characteristics

8 V < V_S < 18 V; INH = High; I_{OUT1-2} = 0 A; – 40 °C < T_j < 150 °C;
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Current Consumption

Quiescent current	I _S	–	20	50	μA	INH = LOW
Quiescent current	I _S	–	20	30	μA	INH = LOW; V _S = 13.2 V; T _j = 25 °C
Supply current	I _S	–	10	20	mA	–
Supply current	I _S	–	–	30	mA	I _{OUT1} = 0.4 A I _{OUT2} = – 0.4 A
Supply current	I _S	–	–	50	mA	I _{OUT1} = 0.8 A I _{OUT2} = – 0.8 A

Over- and Under Voltage Lockout

UV Switch ON voltage	V _{UV ON}	–	6.5	7.5	V	V _S increasing
UV Switch OFF voltage	V _{UV OFF}	5.0	6	–	V	V _S decreasing
UV ON/OFF hysteresis	V _{UV HY}	–	0.5	–	V	V _{UV ON} – V _{UV OFF}
OV Switch OFF voltage	V _{OV OFF}	–	20	24	V	V _S increasing
OV Switch ON voltage	V _{OV ON}	18.0	19.5	–	V	V _S decreasing
OV ON/OFF hysteresis	V _{OV HY}	–	0.5	–	V	V _{OV OFF} – V _{OV ON}

Electrical Characteristics (cont'd)

8 V < V_S < 18 V; INH = High; $I_{OUT1-2} = 0$ A; $-40\text{ °C} < T_j < 150\text{ °C}$;
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Outputs OUT1-2**Saturation Voltages**

Source (upper) $I_{OUT} = -0.2$ A	$V_{SAT\ U}$	–	0.85	1.15	V	$T_j = 25\text{ °C}$
Source (upper) $I_{OUT} = -0.4$ A	$V_{SAT\ U}$	–	0.90	1.20	V	$T_j = 25\text{ °C}$
Sink (upper) $I_{OUT} = -0.8$ A	$V_{SAT\ U}$	–	1.10	1.50	V	$T_j = 25\text{ °C}$
Sink (lower) $I_{OUT} = 0.2$ A	$V_{SAT\ L}$	–	0.15	0.23	V	$T_j = 25\text{ °C}$
Sink (lower) $I_{OUT} = 0.4$ A	$V_{SAT\ L}$	–	0.25	0.40	V	$T_j = 25\text{ °C}$
Sink (lower) $I_{OUT} = 0.8$ A	$V_{SAT\ L}$	–	0.45	0.75	V	$T_j = 25\text{ °C}$

Total Drop	$I_{OUT} = 0.2$ A	V_{SAT}	–	1	1.4	V	$V_{SAT} = V_{SAT\ U} + V_{SAT\ L}$
Total Drop	$I_{OUT} = 0.4$ A	V_{SAT}	–	1.2	1.7	V	$V_{SAT} = V_{SAT\ U} + V_{SAT\ L}$
Total Drop	$I_{OUT} = 0.8$ A	V_{SAT}	–	1.6	2.5	V	$V_{SAT} = V_{SAT\ U} + V_{SAT\ L}$

Clamp Diodes

Forward voltage; upper	V_{FU}	–	1	1.5	V	$I_F = 0.4$ A
Upper leakage current	I_{LKU}	–	–	5	mA	$I_F = 0.4\text{ A}^{1)}$
Forward voltage; lower	V_{FL}	–	0.9	1.4	V	$I_F = 0.4$ A

Notes see page 10.

Electrical Characteristics (cont'd)

8 V < V_S < 18 V; INH = High; I_{OUT1-2} = 0 A; – 40 °C < T_j < 150 °C;
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Input-Interface

Logic Inputs IN1; IN2

H-input voltage	V _{IH}	–	2	3	V	–
L-input voltage	V _{IL}	1	1.5	–	V	–
Hysteresis of input voltage	V _{IHY}	–	0.5	–	V	–
H-input current	I _{IH}	– 2	–	10	μA	V _I = 5 V
L-input current	I _{IL}	– 100	– 20	– 5	μA	V _I = 0 V

Logic Input INH

H-input voltage	V _{IH}	–	2.7	3.5	V	–
L-input voltage	V _{IL}	1	2	–	V	–
Hysteresis of input voltage	V _{IHY}	–	0.7	–	V	–
H-input current	I _{IH}	–	100	250	μA	V _{INH} = 5 V
L-input current	I _{IL}	– 10	–	10	μA	V _{INH} = 0 V

Error-Flag EF

L-output voltage level	V _{EFL}	–	0.2	0.4	V	I _{EF} = 2 mA
Leakage current	I _{EFLK}	–	–	10	μA	0 V < V _{EF} < 7 V

Electrical Characteristics (cont'd)

8 V < V_S < 18 V; INH = High; $I_{OUT1-2} = 0$ A; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$;
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Thermal Shutdown

Thermal shutdown junction temperature	T_{jSD}	150	175	200	$^{\circ}\text{C}$	—
Thermal switch-on junction temperature	T_{jSO}	120	—	170	$^{\circ}\text{C}$	—
Temperature hysteresis	ΔT	—	30	—	K	—

¹⁾ Guaranteed by design.

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25^{\circ}\text{C}$ and the given supply voltage.

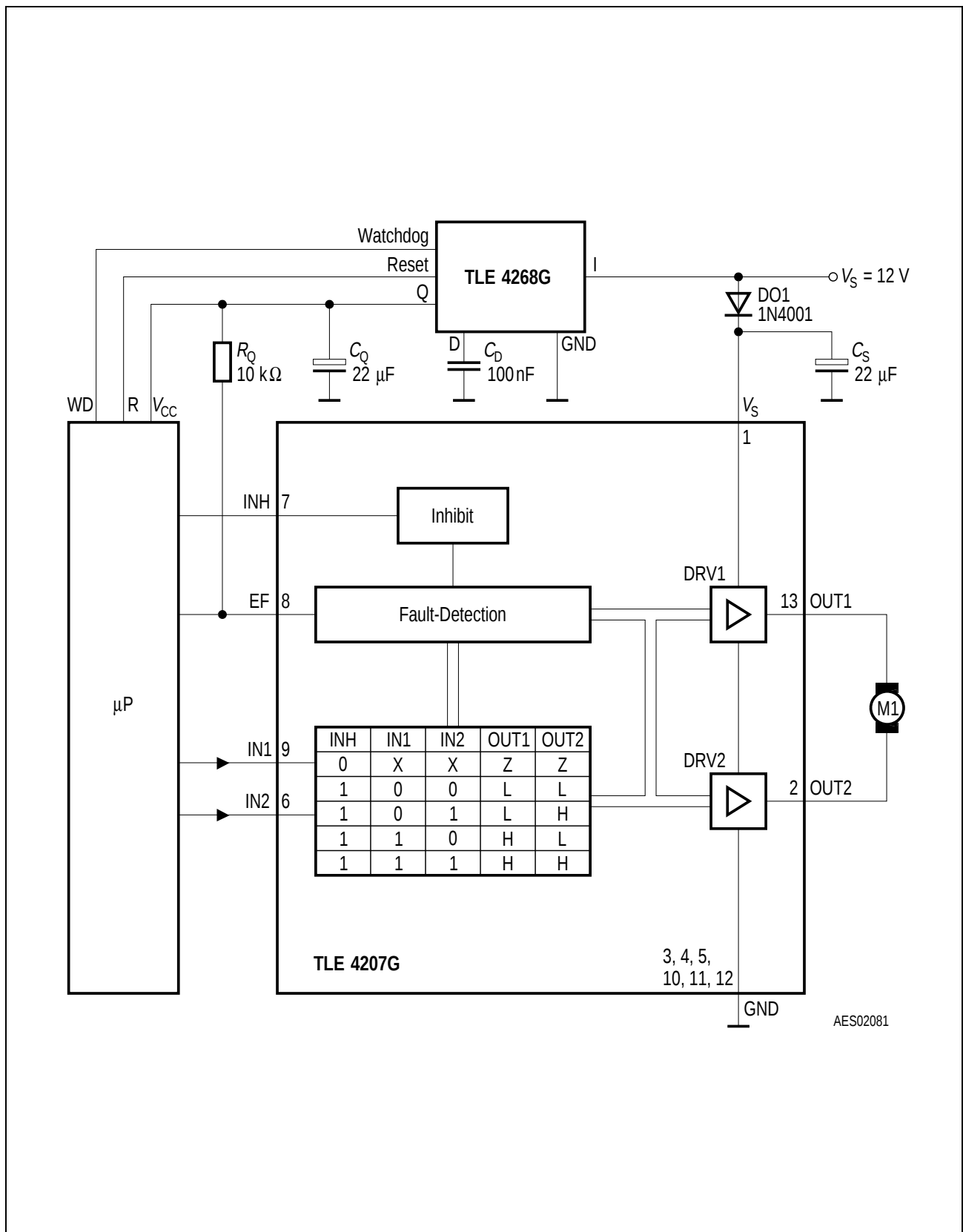
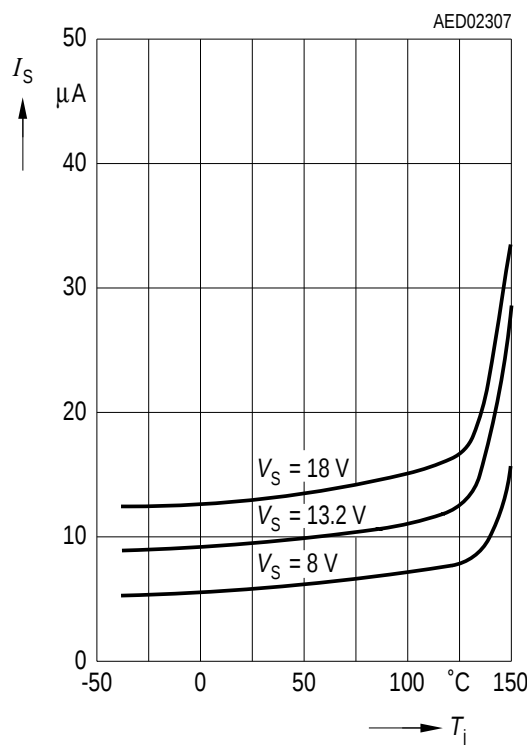


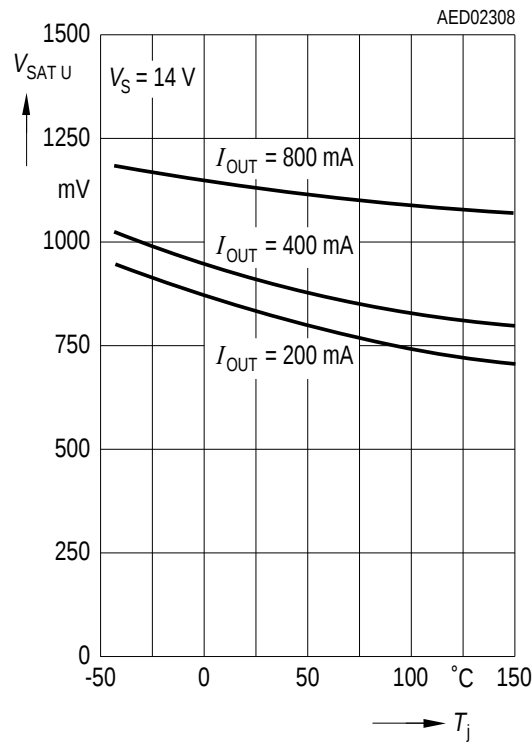
Figure 3 Application Circuit

Diagrams

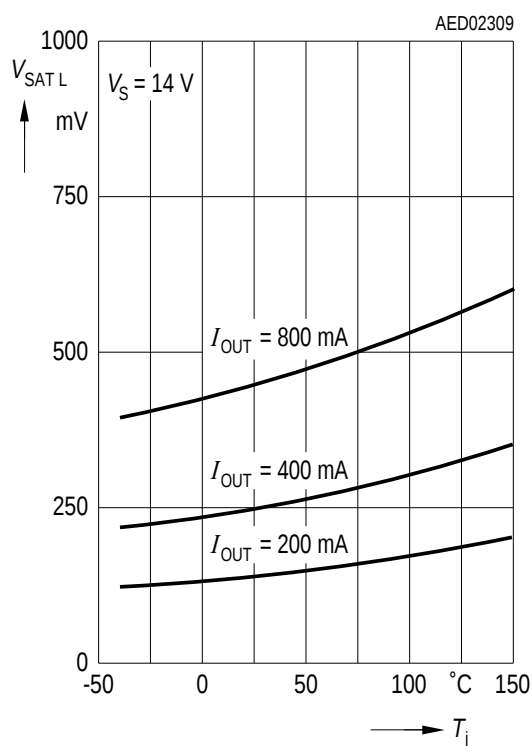
Quiescent current I_S over Temperature



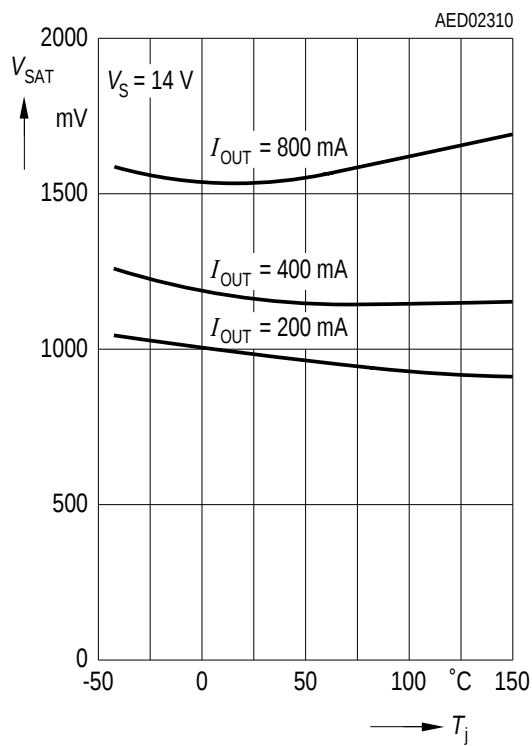
Saturation Voltage of Source $V_{SAT U}$ over Temperature



Saturation Voltage of Sink $V_{SAT L}$ over Temperature

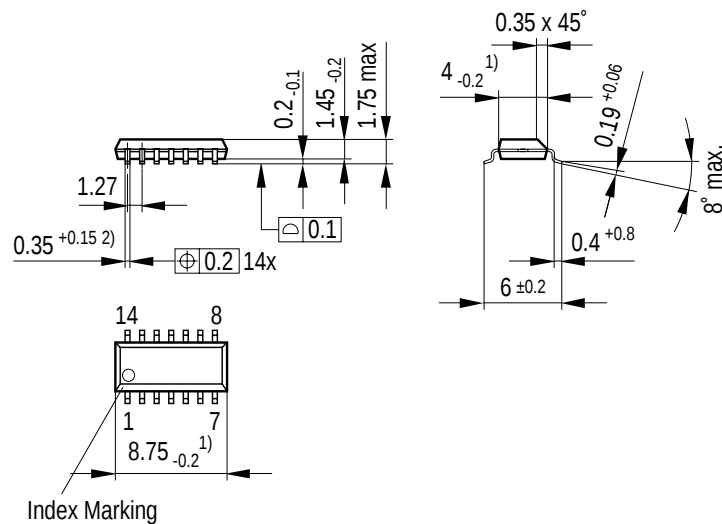


Total Drop at outputs V_{SAT} over Temperature



Package Outlines

P-DSO-14-4
(Plastic Dual Small Outline Package)



- Index Marking
- 1) Does not include plastic or metal protrusion of 0.15 max. per side
 - 2) Does not include dambar protrusion of 0.05 max. per side

GPS05093

Sorts of Packing

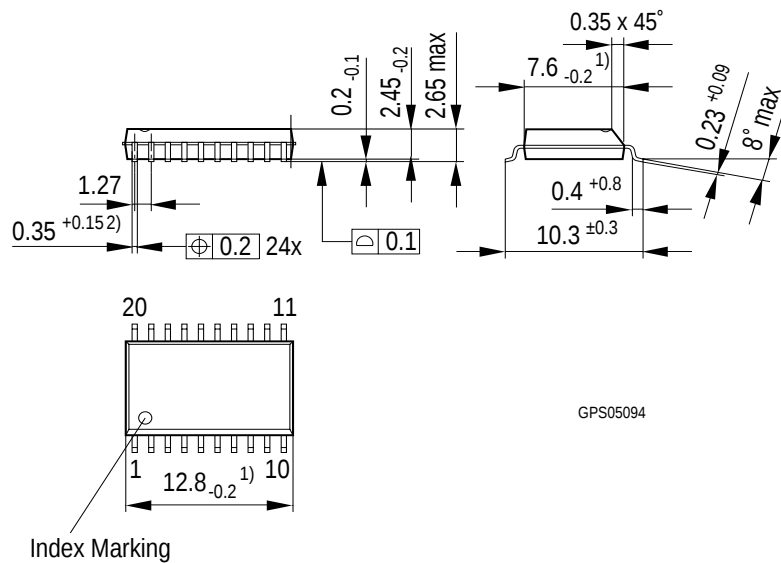
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

P-DSO-20-6

(Plastic Dual Small Outline Package)



- 1) Does not include plastic or metal protrusions of 0.15 max per side
- 2) Does not include dambar protrusion of 0.05 max per side

Sorts of Packing

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