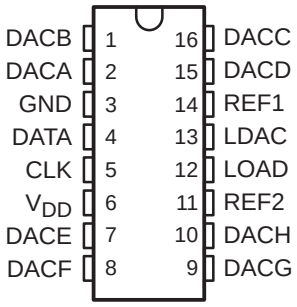
- **Eight 8-Bit Voltage Output DACs**
- **5-V Single-Supply Operation**
- **Serial Interface**
- **High-Impedance Reference Inputs**
- **Programmable 1 or 2 Times Output Range**
- **Simultaneous Update Facility**
- **Internal Power-On Reset**
- **Low-Power Consumption**
- **Half-Buffered Output**

N OR DW PACKAGE
(TOP VIEW)



applications

- **Programmable Voltage Sources**
- **Digitally Controlled Amplifiers/Attenuators**
- **Mobile Communications**
- **Automatic Test Equipment**
- **Process Monitoring and Control**
- **Signal Synthesis**

description

The TLC5628C and TLC5628I are octal 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND and are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

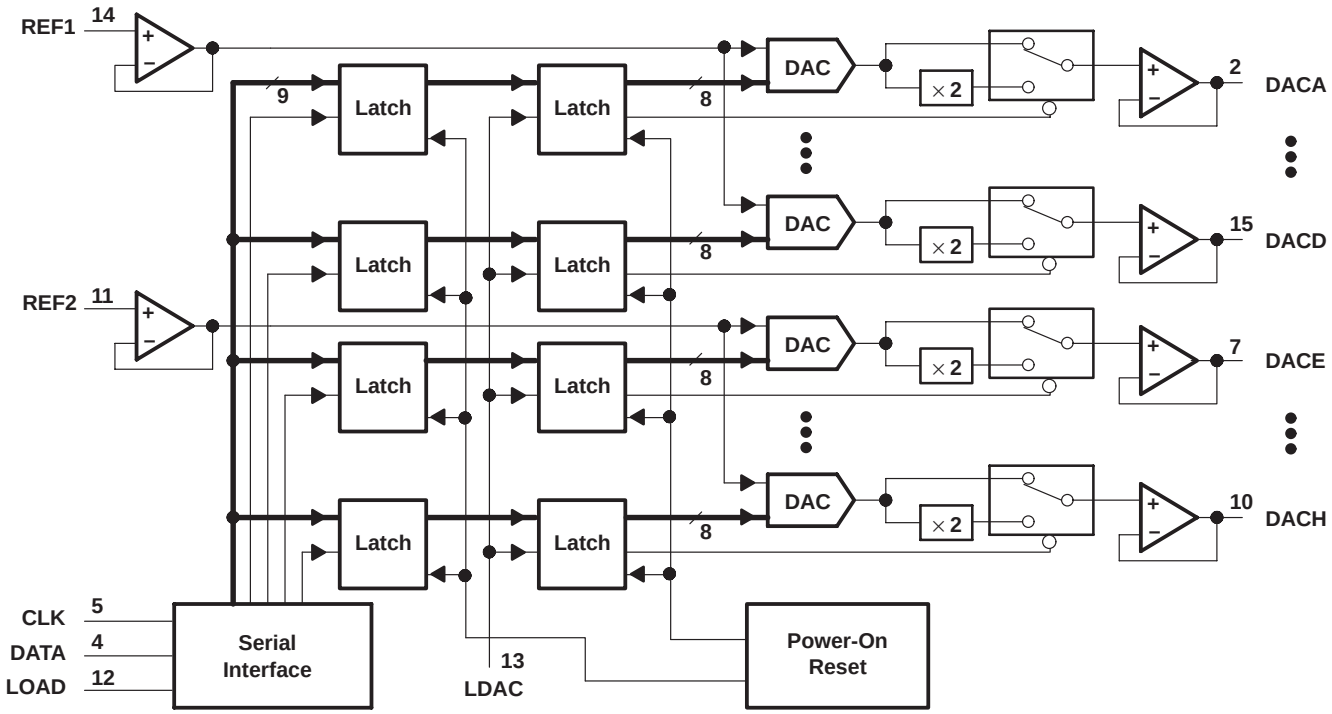
Digital control of the TLC5628C and TLC5628I are over a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 12-bit command word comprises eight bits of data, three DAC select bits, and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs are updated simultaneously through control of LDAC. The digital inputs feature Schmitt triggers for high-noise immunity.

The 16-terminal small-outline (D) package allows digital control of analog functions in space-critical applications. The TLC5628C is characterized for operation from 0°C to 70°C. The TLC5628I is characterized for operation from –40°C to 85°C. The TLC5628C and TLC5628I do not require external trimming.

AVAILABLE OPTIONS

	PACKAGE	
T_A	SMALL OUTLINE (DW)	PLASTIC DIP (N)
0°C to 70°C	TLC5628CDW	TLC5628CN
–40°C to 85°C	TLC5628IDW	TLC5628IN

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	5	I	Serial interface clock. The input digital data is shifted into the serial interface register on the falling edge of the clock applied to the CLK terminal.
DACA	2	O	DAC A analog output
DACB	1	O	DAC B analog output
DACC	16	O	DAC C analog output
DACD	15	O	DAC D analog output
DACE	7	O	DAC E analog output
DACF	8	O	DAC F analog output
DACG	9	O	DAC G analog output
DACH	10	O	DAC H analog output
DATA	4	I	Serial interface digital data input. The digital code for the DAC is clocked into the serial interface register serially. Each data bit is clocked into the register on the falling edge of the clock signal.
GND	3	I	Ground return and reference terminal
LDAC	13	I	Load DAC. When LDAC is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is taken from high to low.
LOAD	12	I	Serial interface load control. When LDAC is low, the falling edge of the LOAD signal latches the digital data into the output latch and immediately produces the analog voltage at the DAC output terminal.
REF1	14	I	Reference voltage input to DAC A|B|C|D. This voltage defines the analog output range.
REF2	11	I	Reference voltage input to DAC E|F|G|H. This voltage defines the analog output range.
V_{DD}	6	I	Positive supply voltage

detailed description

The TLC5628 is implemented using eight resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to GND and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor segments and upon the performance of the output buffer. Since the inputs are buffered, the DACs always present a high-impedance load to the reference sources. There are two input reference terminals; REF1 is used for DACA through DACD and REF2 is used by DACE through DACH.

Each DAC output is buffered by a configurable-gain output amplifier, that can be programmed to times 1 or times 2 gain.

On power up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA|B|C|D|E|F|G|H}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial control word.

Table 1. Ideal Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated when LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered most significant bit (MSB) first. Data transfers using two 8-clock cycle periods are shown in Figures 3 and 4.

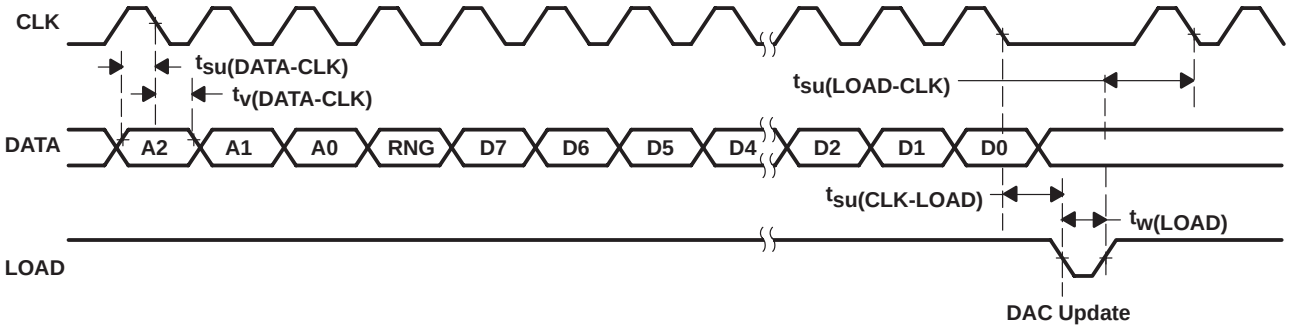


Figure 1. LOAD-Controlled Update (LDAC = Low)

data interface (continued)

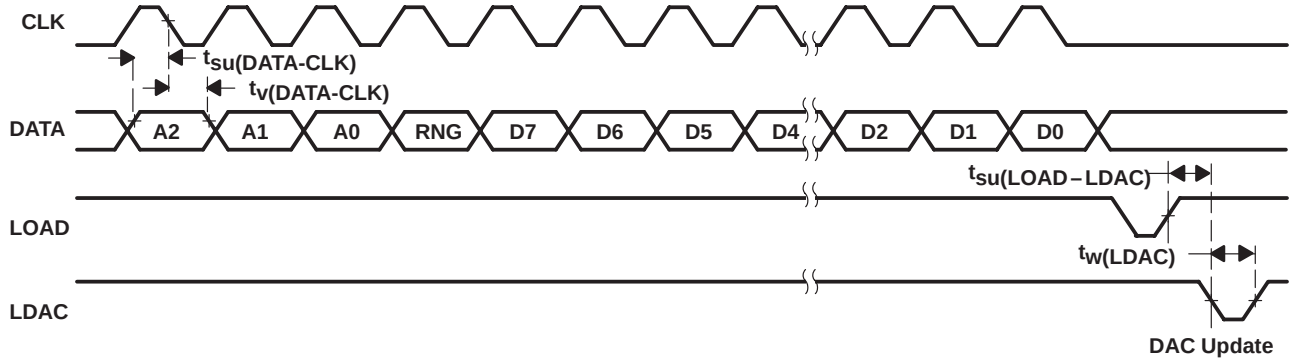


Figure 2. LDAC-Controlled Update

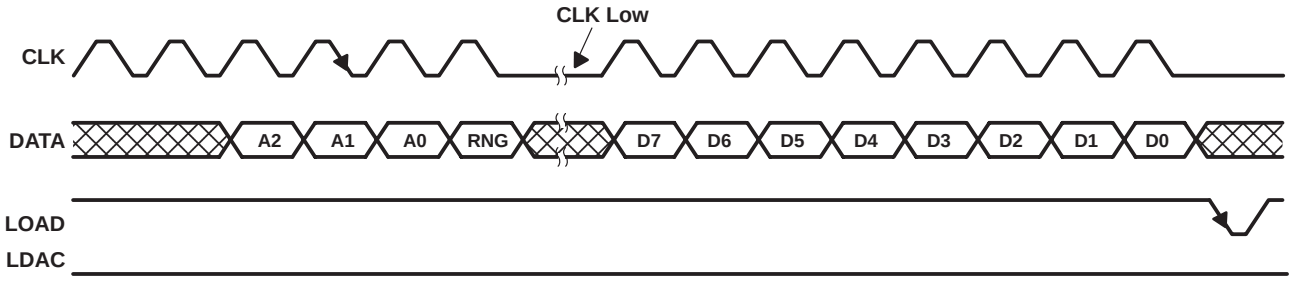


Figure 3. Load-Controled Update Using 8-Bit Serial Word (LDAC = Low)

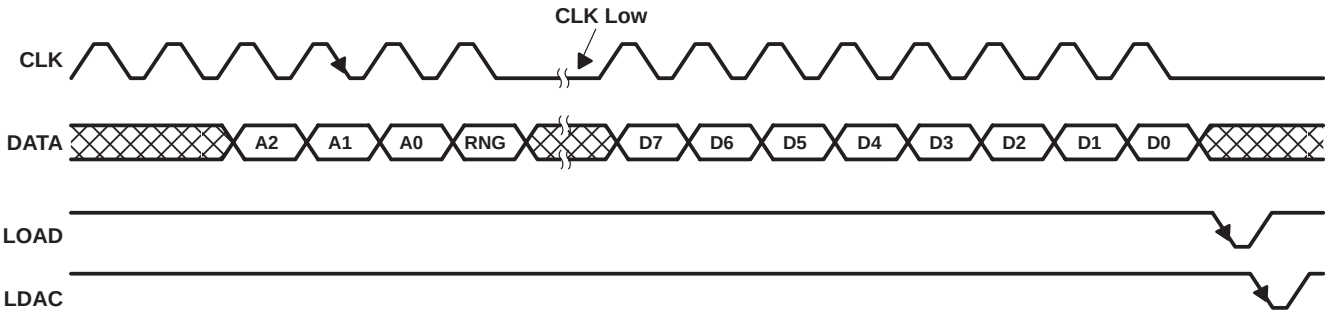


Figure 4. LDAC-Controlled Update Using 8-Bit Serial Word

Table 2 lists the A2, A1, and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 2. Serial Input Decode

A2	A1	A0	DAC UPDATED
0	0	0	DACA
0	0	1	DACB
0	1	0	DACC
0	1	1	DACD
1	0	0	DACE
1	0	1	DACF
1	1	0	DACG
1	1	1	DACH

linearity, offset, and gain error using single-end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset voltage, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, therefore, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground.

The output voltage remains at 0 V until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in the transfer function shown in Figure 5.

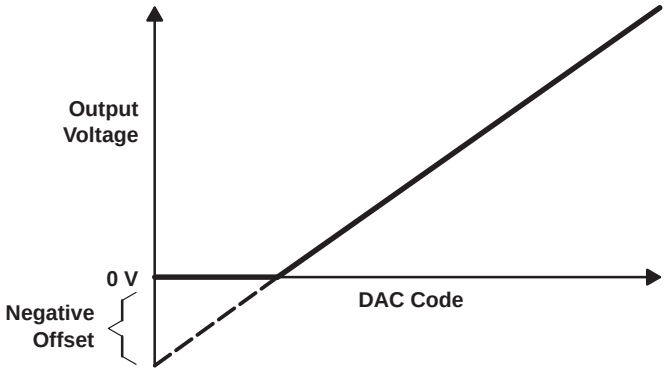


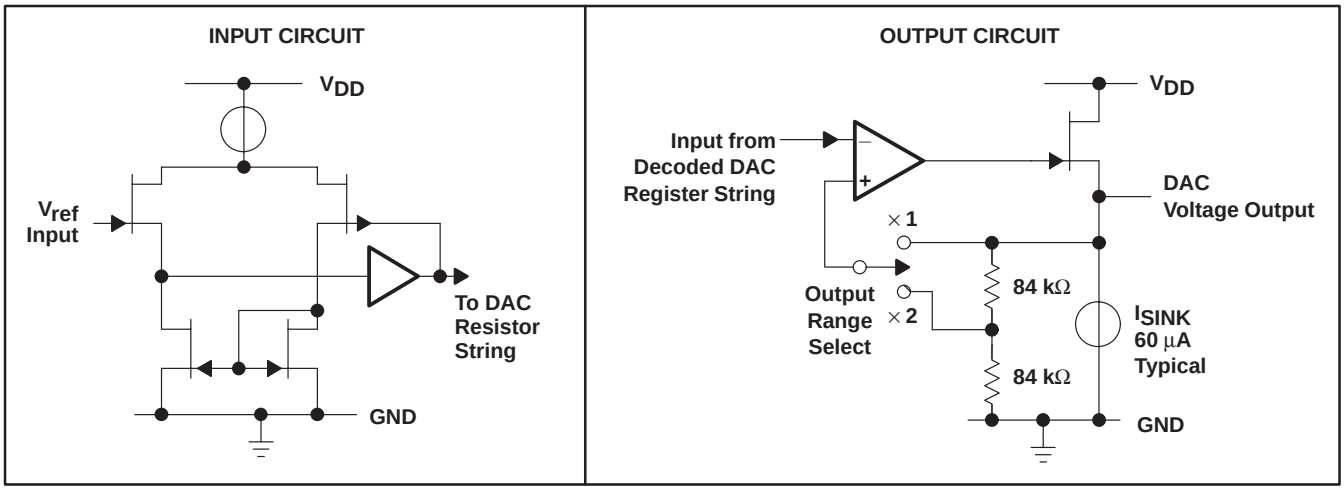
Figure 5. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces the breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

For a DAC, linearity is measured between the zero-input code (all inputs are 0) and the full-scale code (all inputs are 1) after offset and full scale are adjusted out or accounted for in some way. However, single-supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity in the unipolar mode is measured between full-scale code and the lowest code that produces a positive output voltage.

The code is calculated from the maximum specification for the negative offset voltage.

equivalent of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND) . . . . . 7 V
Digital input voltage range, V_{ID} . . . . . GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range . . . . . GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLC5628C . . . . . 0°C to 70°C
TLC5628I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75		5.25	V
High-level voltage, V_{IH}		0.8 V_{DD}			V
Low-level voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} [A|B|C|D|E|F|G|H]				V_{DD}–1.5	V
Analog full-scale output voltage, R_L = 10 kΩ			3.5		V
Load resistance, R_L		10			kΩ
Setup time, data input, $t_{su(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Valid time, data input valid after CLK↓, $t_{v(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Setup time, CLK eleventh falling edge to LOAD, $t_{su(CLK-LOAD)}$ (see Figure 1)		50			ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD-CLK)}$ (see Figure 1)		50			ns
Pulse duration, LOAD, $t_{w(LOAD)}$ (see Figure 1)		250			ns
Pulse duration, LDAC, $t_{w(LDAC)}$ (see Figure 2)		250			ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$ (see Figure 2)		0			ns
CLK frequency				1	MHz
Operating free-air temperature, T_A	TLC5628C	0		70	°C
	TLC5628I	–40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	$V_I = V_{DD}$				±10	µA
I_{IL}	Low-level input current	V_I = 0 V				±10	µA
$I_{O(sink)}$	Output sink current	Each DAC output		20			µA
$I_{O(source)}$	Output source current			2			mA
C_i	Input capacitance				15		pF
	Reference input capacitance				15		
I_{DD}	Supply current	V_{DD} = 5 V				4	mA
I_{ref}	Reference input current	V_{DD} = 5 V,	V_{ref} = 2 V			±10	µA
E_L	Linearity error (end point corrected)	V_{ref} = 2 V,	× 2 gain (see Note 1)			±1	LSB
E_D	Differential-linearity error	V_{ref} = 2 V,	× 2 gain (see Note 2)			±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 2 V,	× 2 gain (see Note 3)	0		30	mV
	Zero-scale-error temperature coefficient	V_{ref} = 2 V,	× 2 gain (see Note 4)		10		µV/°C
E_{FS}	Full-scale error	V_{ref} = 2 V,	× 2 gain (see Note 5)			±60	mV
	Full-scale-error temperature coefficient	V_{ref} = 2 V,	× 2 gain (see Note 6)		±25		µV/°C
PSRR	Power supply rejection ratio	See Notes 7 and 8			0.5		mV/V

NOTES:
1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale-error temperature coefficient is given by: ZSETC = $[ZSE(T_{max}) – ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output (V_{ref} – 1 LSB) with an output load of 10 kΩ.
6. Full-scale error temperature coefficient is given by: FSETC = $[FSE(T_{max}) – FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.
7. Zero-scale-error rejection ratio (ZSE RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Full-scale-error rejection ratio (FSE RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C_L = 100 pF, R_L = 10 kΩ		1		V/µs
Output settling time	To ±0.5 LSB, C_L = 100 pF, R_L = 10 kΩ, See Note 9		10		µs
Large signal bandwidth	Measured at –3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACD		–50		dB
Reference feedthrough	See Note 10		–60		dB
Channel-to-channel isolation	See Note 11		–60		dB
Reference input bandwidth	See Note 12		100		kHz

NOTES:
9. Settling time is the time between a LOAD falling edge and the DAC output reaching full-scale voltage within ±0.5 LSB starting from an initial output voltage equal to zero.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
12. Reference bandwidth is the –3 dB bandwidth with an input at V_{ref} = 1.25 V dc + 2 V_{pp} and with a full-scale digital input code.

PARAMETER MEASUREMENT INFORMATION

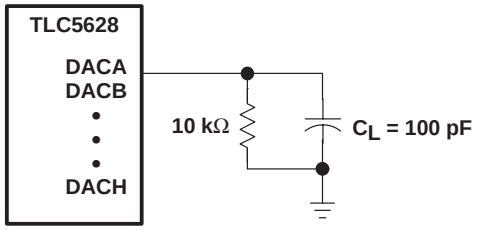


Figure 6. Slew, Settling Time, and Linearity Measurements

TYPICAL CHARACTERISTICS

POSITIVE RISE AND SETTLING TIME

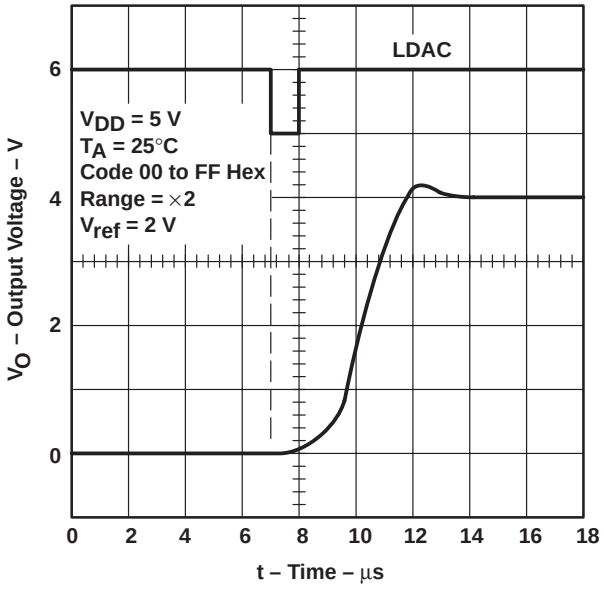


Figure 7

NEGATIVE FALL AND SETTLING TIME

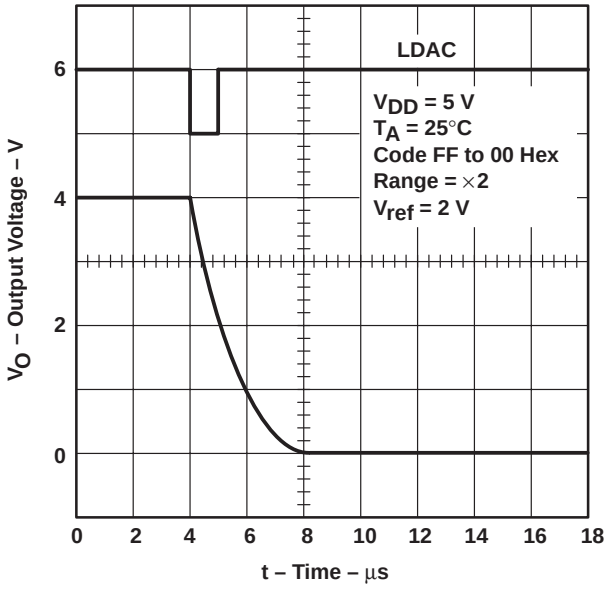


Figure 8

TYPICAL CHARACTERISTICS

DAC OUTPUT VOLTAGE vs OUTPUT LOAD

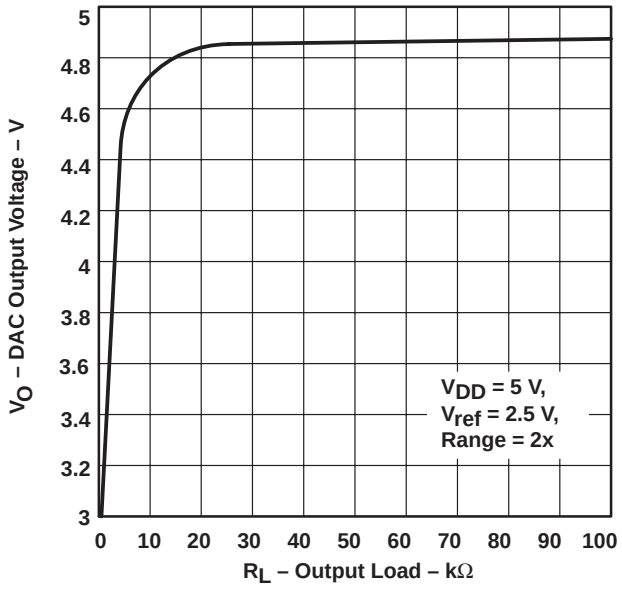


Figure 9

DAC OUTPUT VOLTAGE vs OUTPUT LOAD

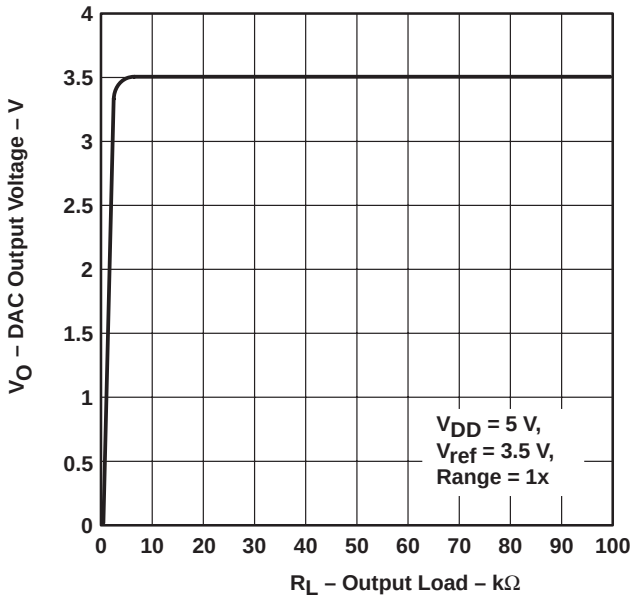


Figure 10

OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

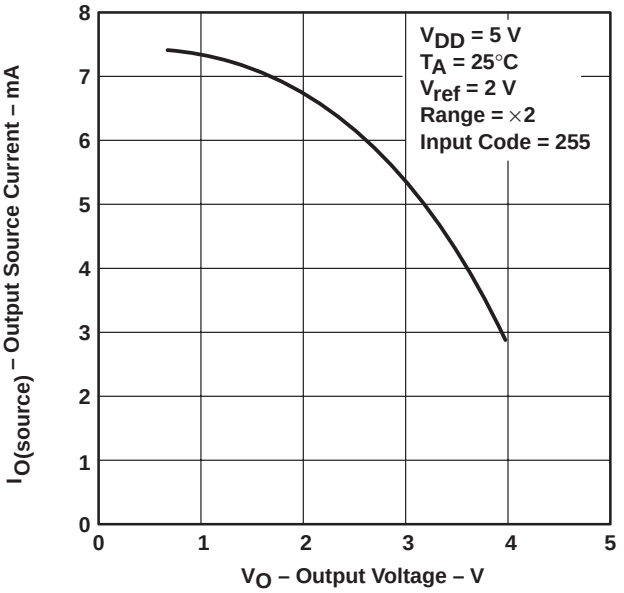


Figure 11

SUPPLY CURRENT vs TEMPERATURE

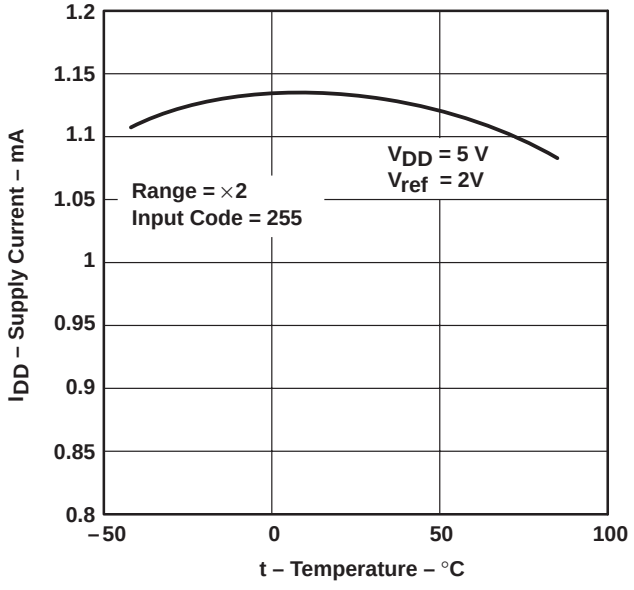


Figure 12

TYPICAL CHARACTERISTICS

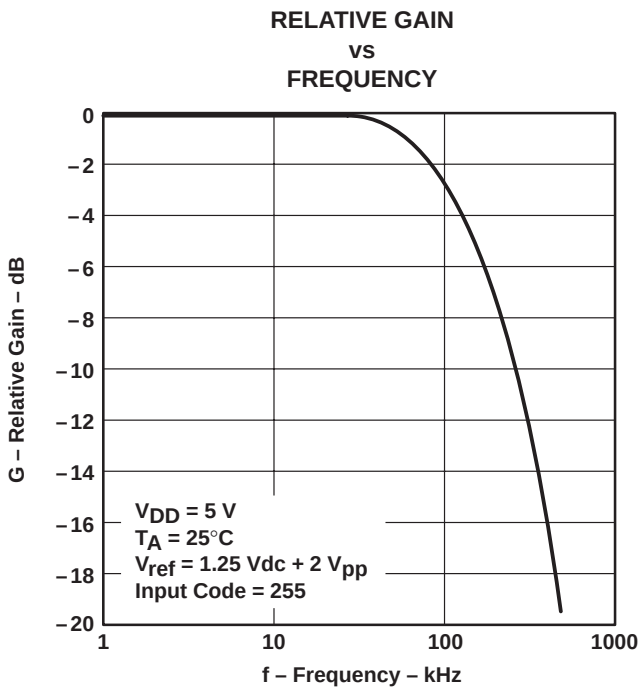


Figure 13

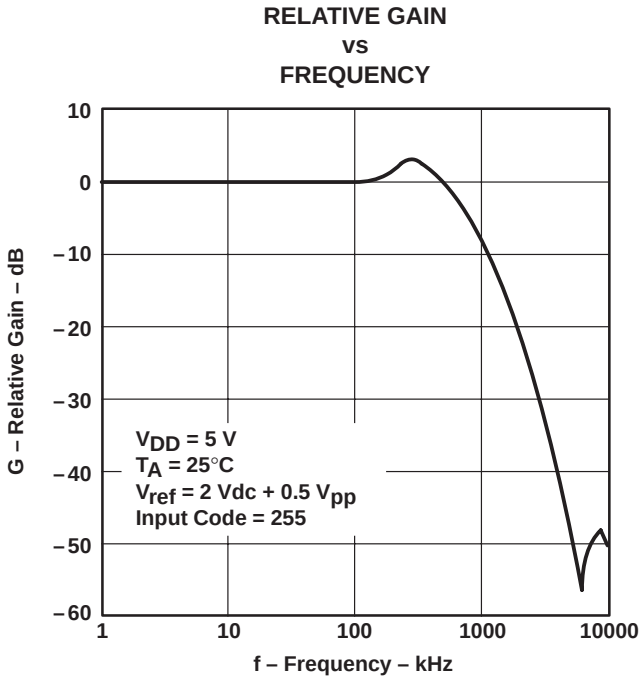
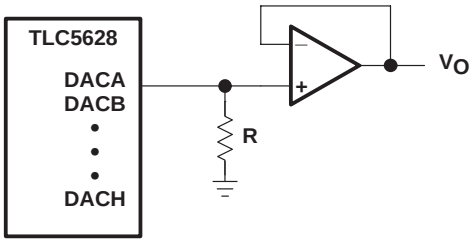


Figure 14

APPLICATION INFORMATION



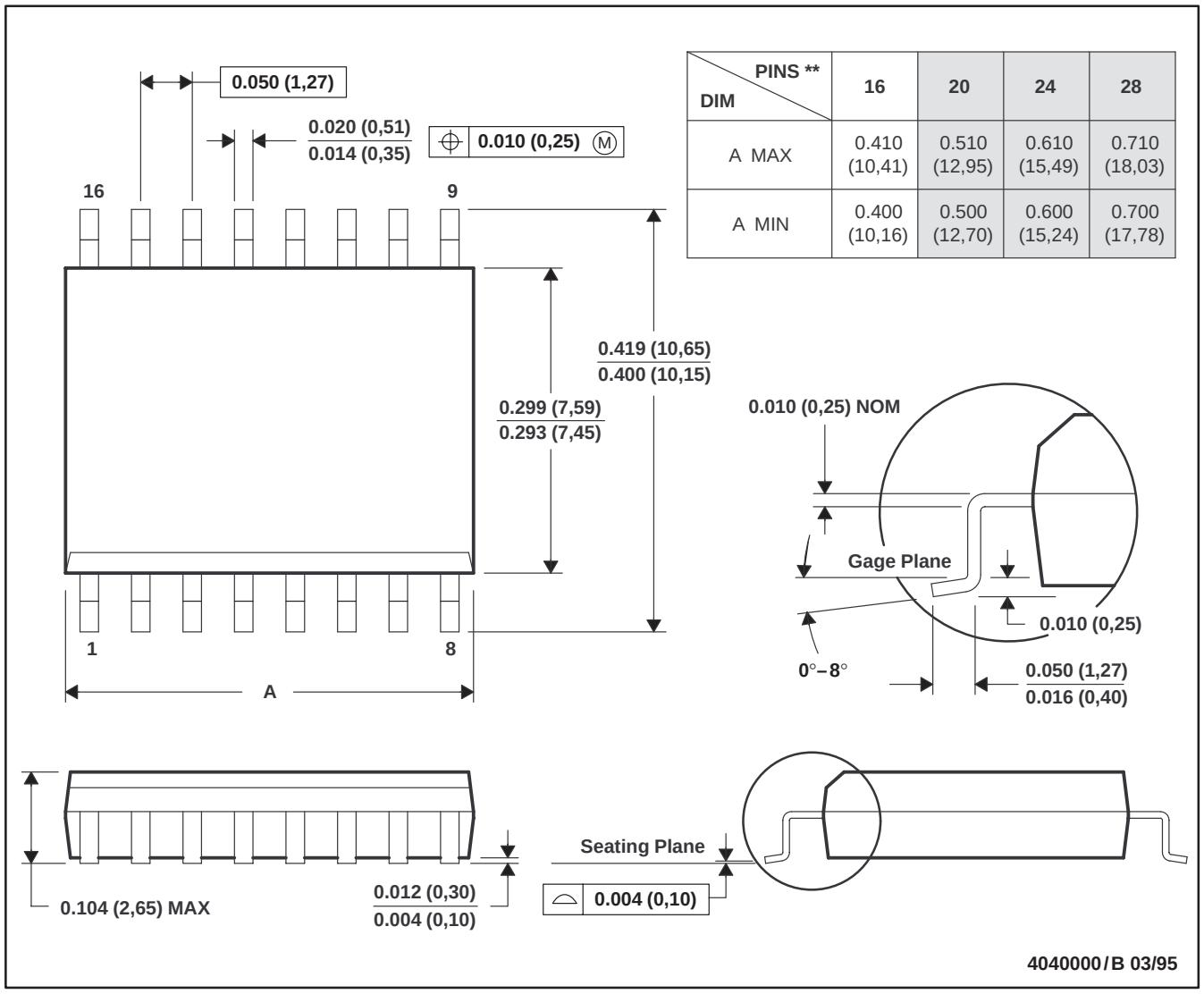
NOTE A: Resistor R ≥ 10 kΩ

Figure 15. Output Buffering Scheme

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

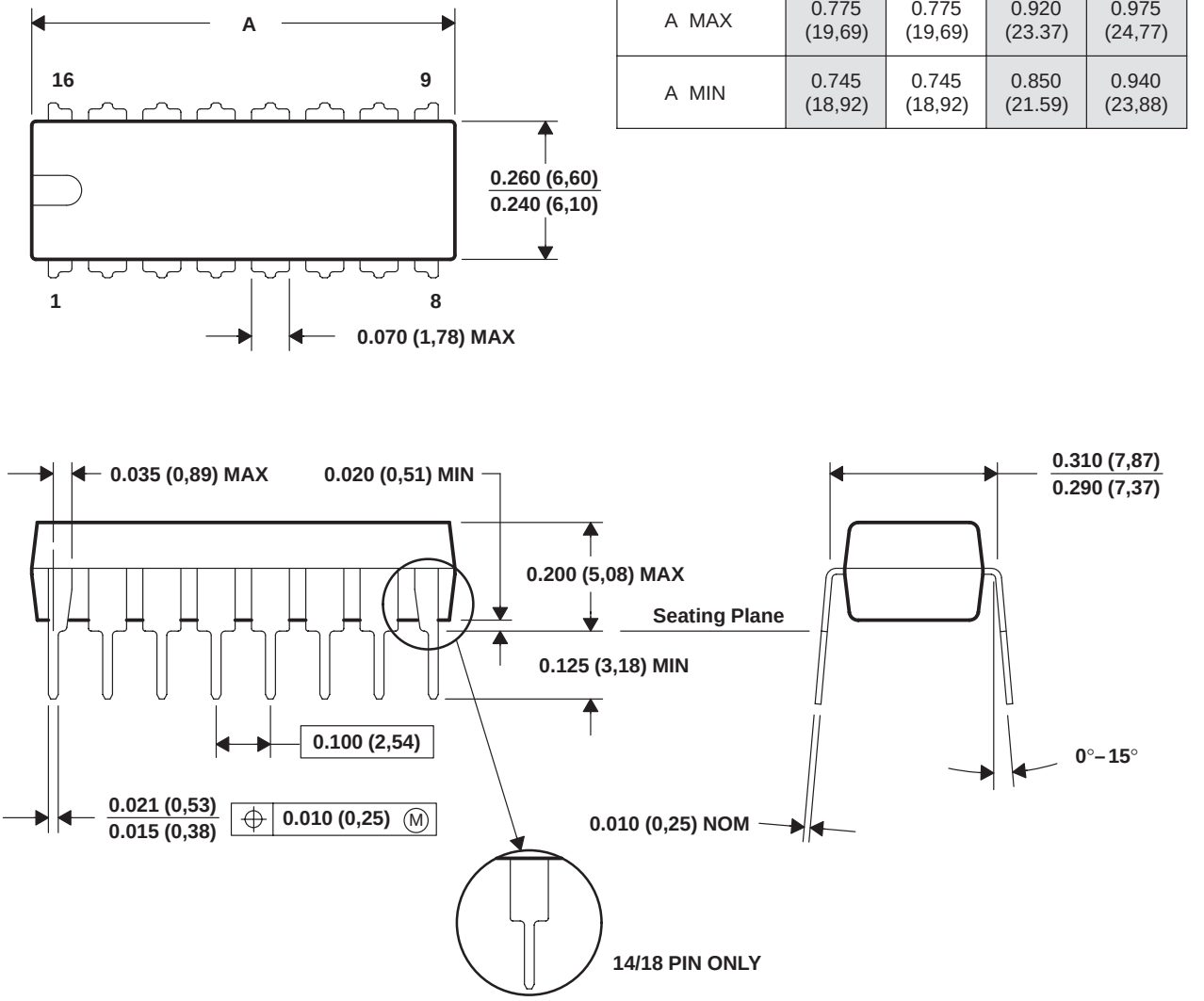
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLC5628CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5628CDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5628CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5628CDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5628CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type
TLC5628CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type
TLC5628IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5628IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5628IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5628IDWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5628IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type
TLC5628INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

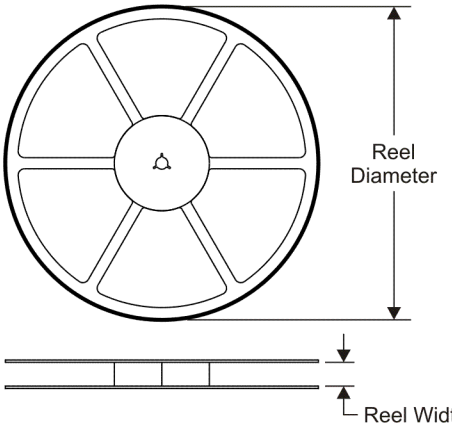
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

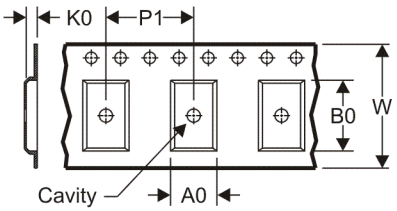
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

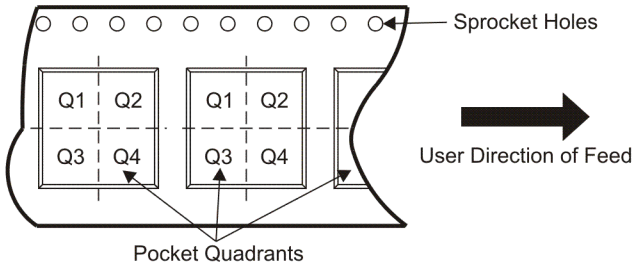


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

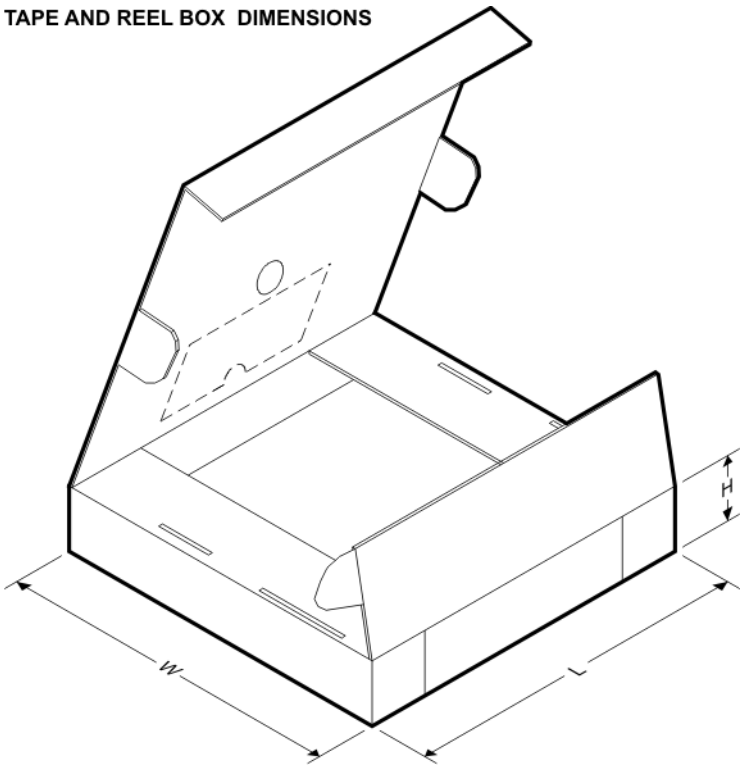
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5628CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TLC5628IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5628CDWR	SOIC	DW	16	2000	346.0	346.0	33.0
TLC5628IDWR	SOIC	DW	16	2000	346.0	346.0	33.0

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