

## P-channel 30 V, 0.048 $\Omega$ typ., 4 A STripFET™ H6 DeepGATE™ Power MOSFET in PowerFLAT™ 2x2 package

Datasheet - preliminary data

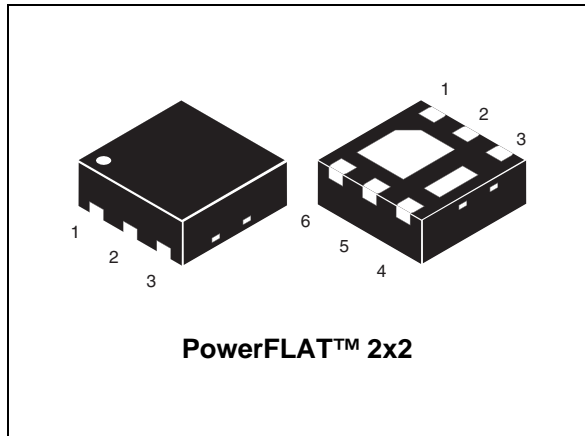
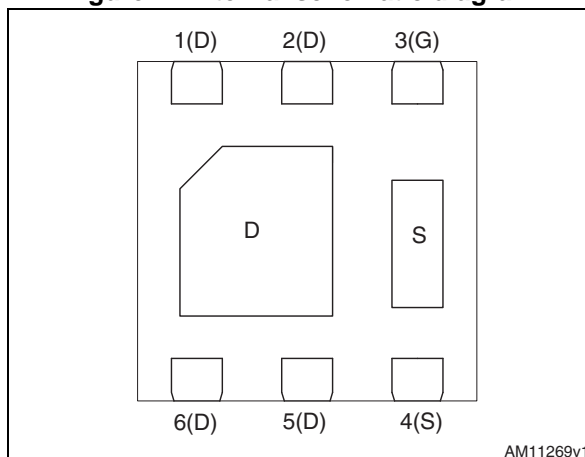


Figure 1. Internal schematic diagram



### Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL4P3LLH6	30 V	0.056 $\Omega$ at 10 V	4 A

- Very low on-resistance R<sub>DS(on)</sub>
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching application

### Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL4P3LLH6	4K3L	PowerFLAT™ 2x2	Tape and reel

Note: For the P-channel MOSFET the actual polarity of the voltages and the current must be reversed.

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>12</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	4	A
$I_D$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	2.75	A
$I_{DM}^{(1)}$	Drain current (pulsed)	16	A
$P_{TOT}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.4	W
$T_J$	Operating junction temperature	150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	52	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec

*Note:* For the P-channel MOSFET the actual polarity of the voltages and the current must be reversed.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$ , $T_J = 125\text{ °C}$			10	
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2\text{ A}$		0.048	0.056	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 2\text{ A}$		0.075	0.09	

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	639	-	$\mu\text{F}$
$C_{oss}$	Output capacitance		-	79	-	
$C_{rss}$	Reverse transfer capacitance		-	52	-	
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 4\text{ A}$ , $V_{GS} = 4.5\text{ V}$	-	6	-	nC
$Q_{gs}$	Gate-source charge		-	1.9	-	
$Q_{gd}$	Gate-drain charge		-	2.1	-	

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$ , $I_D = 4\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	5.4	-	ns
$t_r$	Rise time		-	5	-	
$t_{d(off)}$	Turn-off delay time		-	19.2	-	
$t_f$	Fall time		-	3.4	-	

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 4 \text{ A}$ , $V_{GS} = 0$	-	-	1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 4 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 16 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$	-	11.2	-	ns
$Q_{rr}$	Reverse recovery charge		-	3.5	-	nC
$I_{RRM}$	Reverse recovery current		-	0.6	-	A

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

*Note:* For the P-channel MOSFET the actual polarity of the voltages and the current must be reversed.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

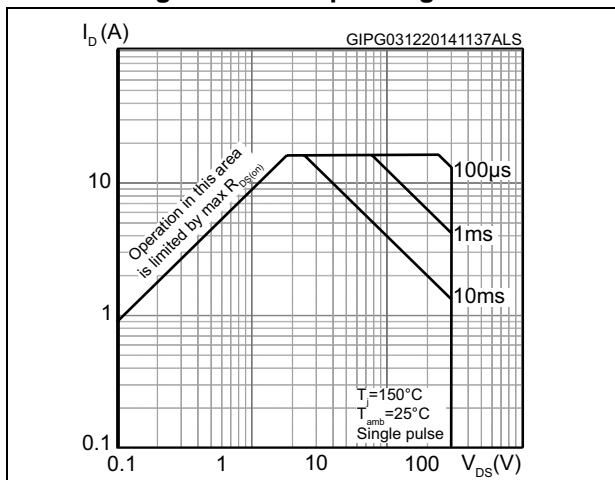


Figure 3. Thermal impedance

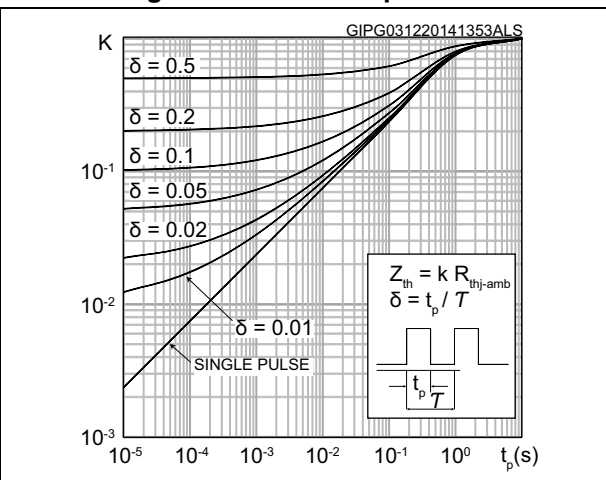


Figure 4. Output characteristics

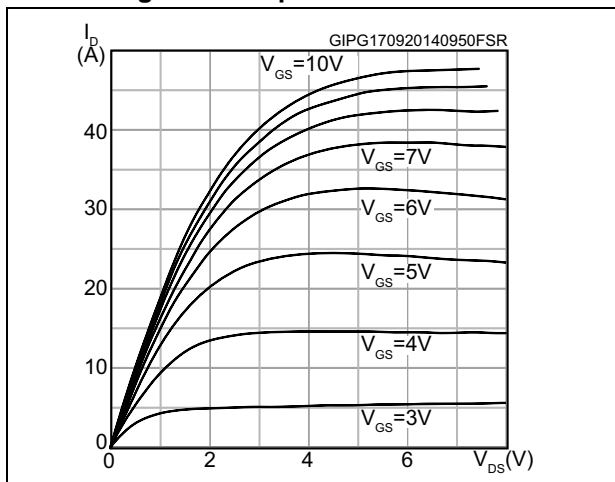


Figure 5. Transfer characteristics

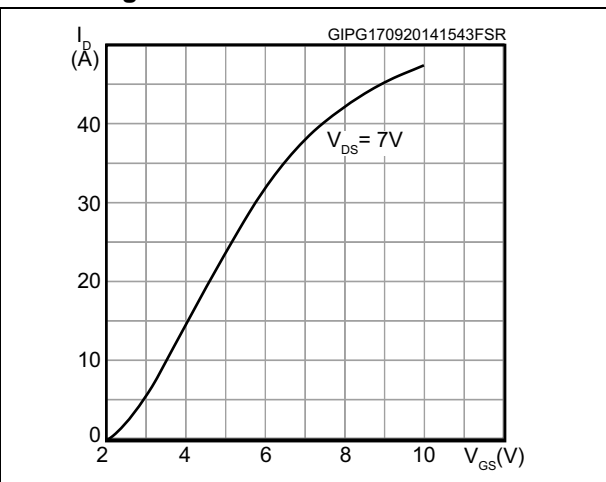


Figure 6. Gate charge vs gate-source voltage

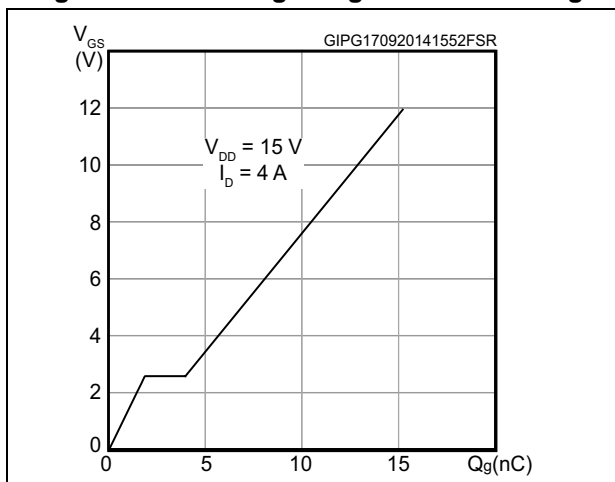


Figure 7. Static drain-source on-resistance

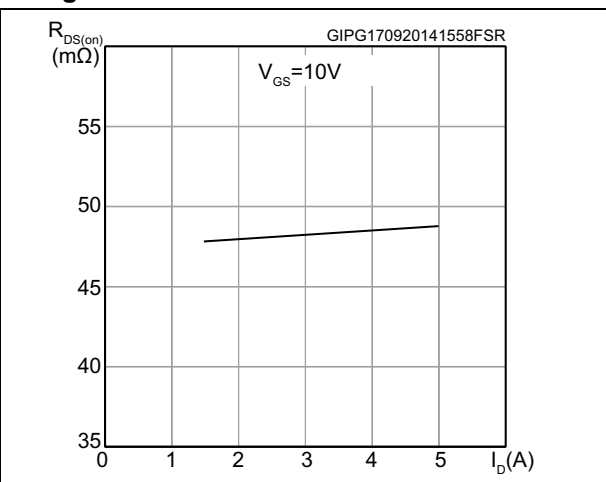


Figure 8. Normalized  $V_{(BR)DSS}$  vs temperature

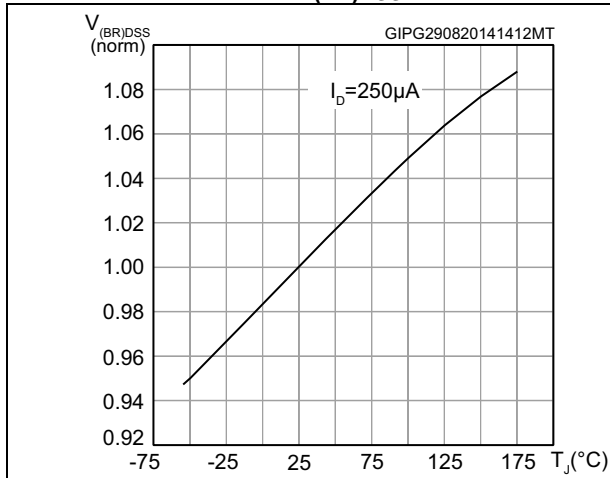


Figure 9. Capacitance variations

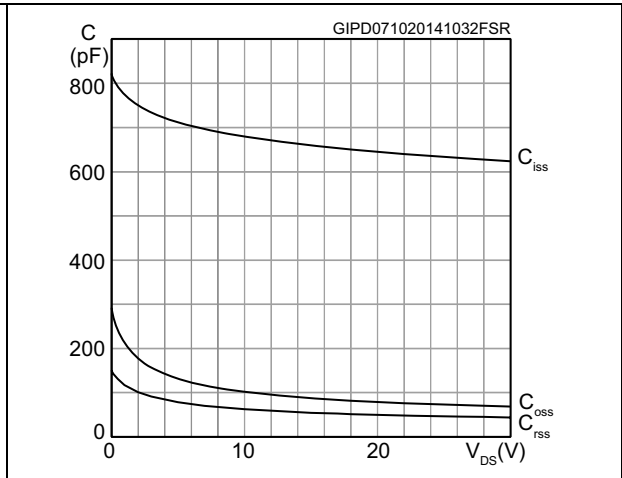


Figure 10. Normalized gate threshold voltage vs. temperature

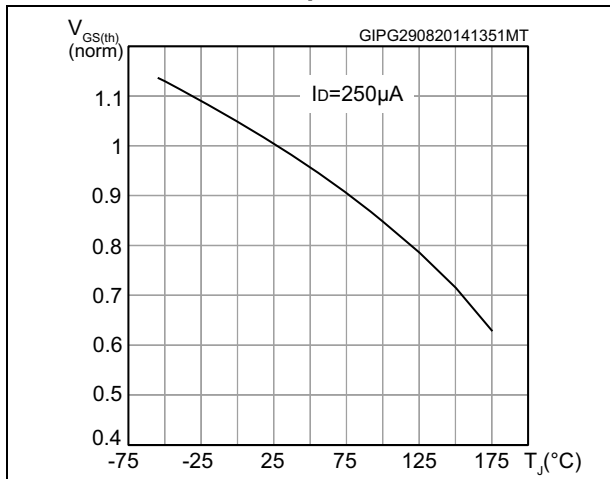


Figure 11. Normalized on-resistance vs. temperature

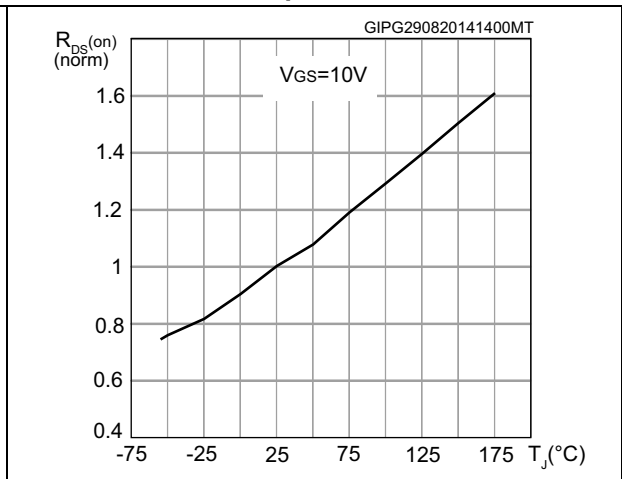
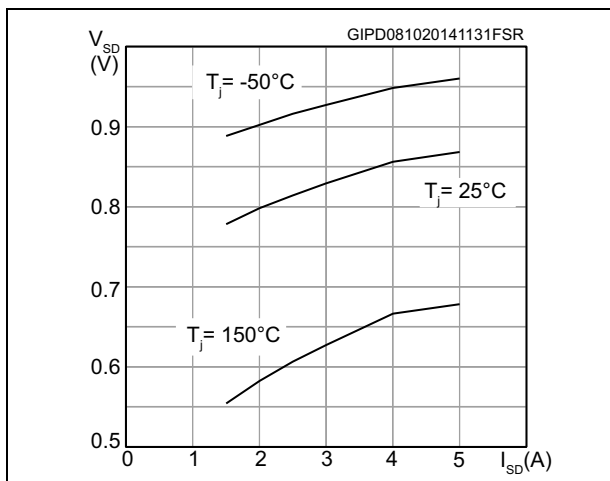


Figure 12. Source-drain diode forward characteristics



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

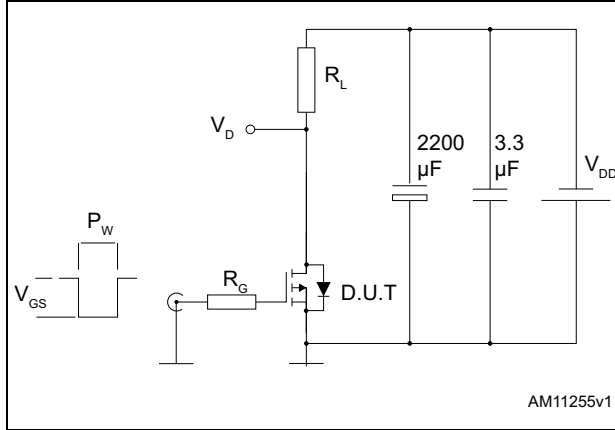


Figure 14. Gate charge test circuit

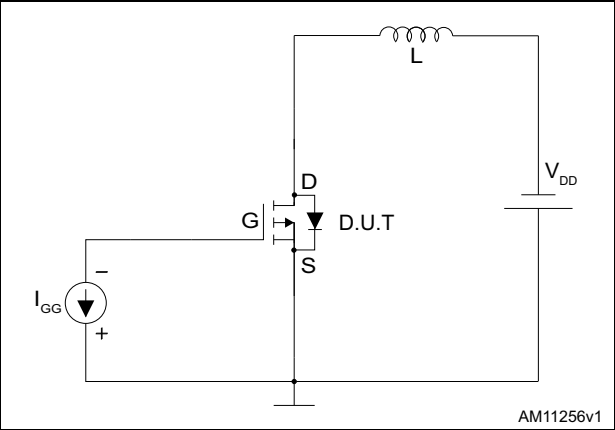
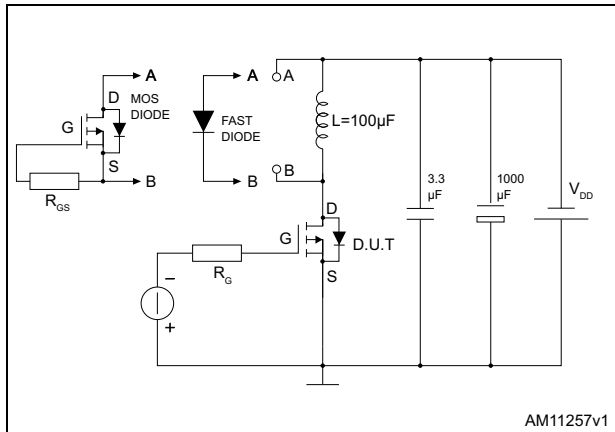


Figure 15. Test circuit for inductive load switching and diode recovery times





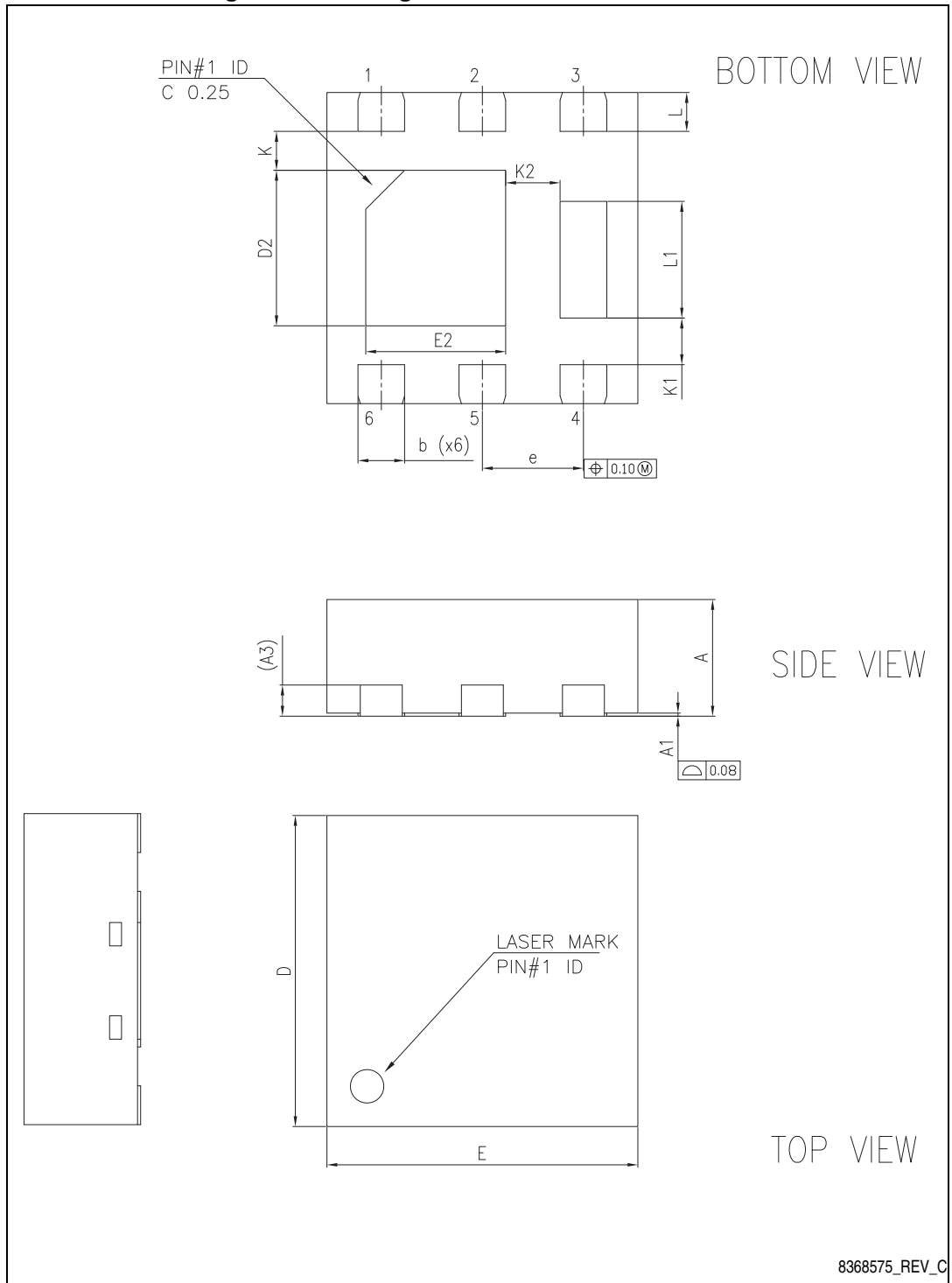
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Table 8. PowerFLAT™ 2 x 2 mechanical data**

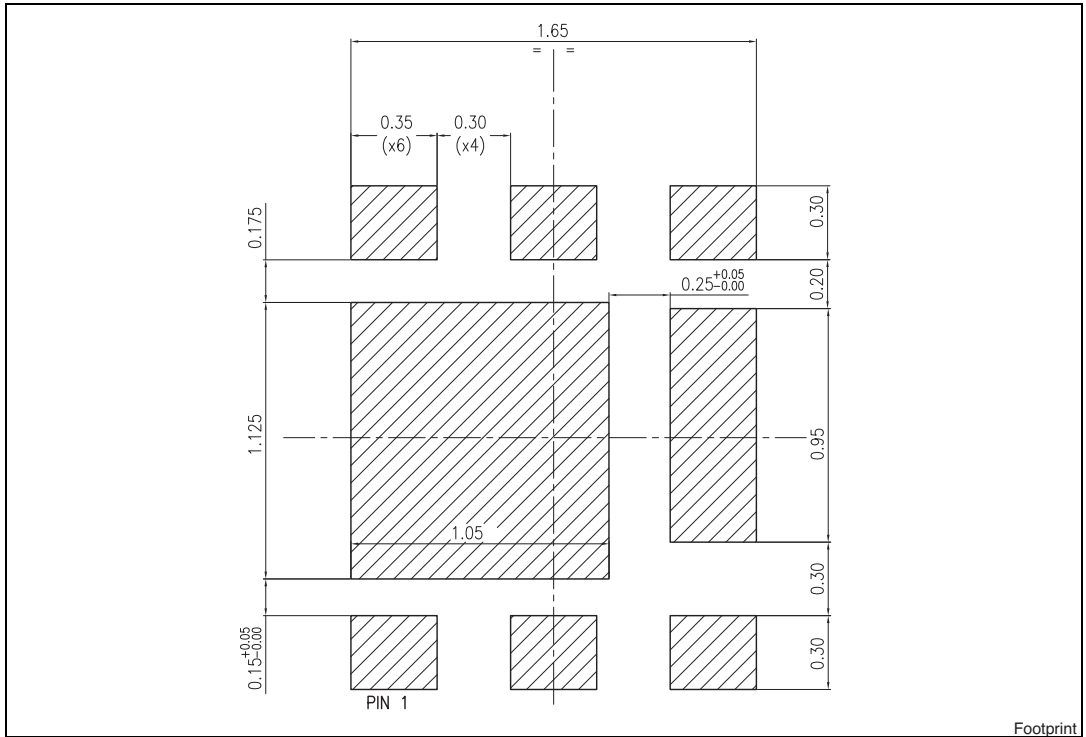
Dim.	mm.		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	0.80	0.90	1.00
e	0.55	0.65	0.75
K	0.15	0.25	0.35
K1	0.20	0.30	0.40
K2	0.25	0.35	0.45
L	0.20	0.25	0.30
L1	0.65	0.75	0.85

Figure 16. Drawing dimension PowerFLAT™ 2 x 2



# 5 Packaging mechanical data

Figure 17. PowerFLAT™ 2 x 2 footprint (dimensions in mm)



## 6 Revision history

Table 9. Document revision history

Date	Revision	Changes
09-May-2013	1	Initial release.
09-Dec-2014	2	Text edits throughout document On cover page: – changed title description – updated features and description In <a href="#">Table 4</a> , changed $R_{DS(on)}$ values In <a href="#">Table 5</a> , changed values and test conditions In <a href="#">Table 6</a> , changed values and test conditions In <a href="#">Table 7</a> , changed values and test conditions Added <a href="#">Section 2.1: Electrical characteristics (curves)</a> Updated <a href="#">Section 3: Test circuits</a> Updated <a href="#">Section 4: Package mechanical data</a>

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