

N-channel 80 V, 3.7 mΩ typ., 120 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

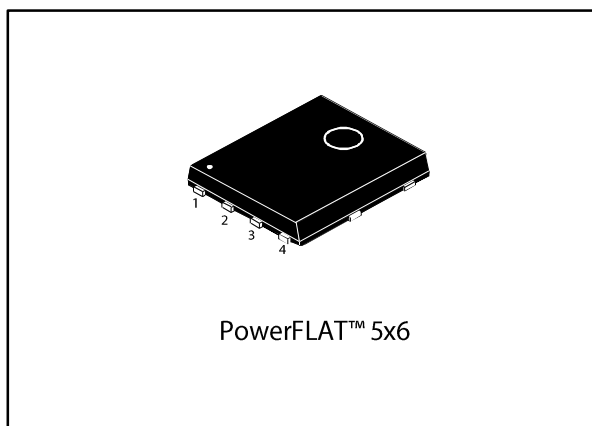
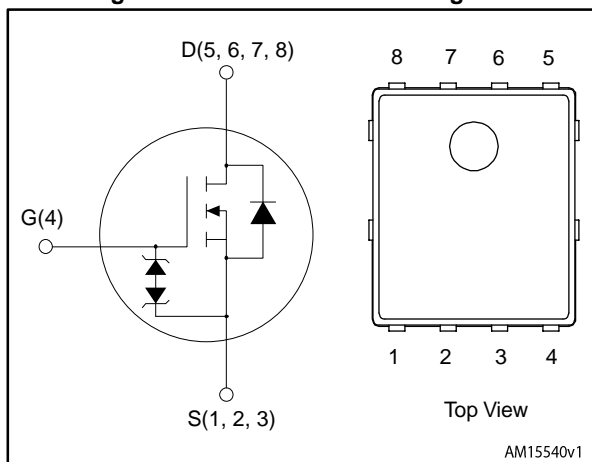


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL120N8F7	80 V	4.4 mΩ	120 A	140 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL120N8F7	120N8F7	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	120	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	90	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	480	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	23	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^{\circ}\text{C}$	17	
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	92	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	140	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{pcb} = 25\text{ }^{\circ}\text{C}$	4.8	W
T_{stg}	Storage temperature	-55 to 175	$^{\circ}\text{C}$
T_j	Operating junction temperature		

Notes:

- (1) This value is rated according to R_{thj-c} .
 (2) Pulse width is limited by safe operating area.
 (3) This value is rated according to $R_{thj-pcb}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	$^{\circ}\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case	1.05	

Notes:

- (1) When mounted on a 1-inch² FR-4 board, 2oz Cu, $t < 10\text{ s}$

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	80			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 80\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = 20\text{ V}$			100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	2		4	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 11.5\text{ A}$		3.7	4.4	$\text{m}\Omega$

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	4570	-	pF
C_{oss}	Output capacitance		-	800	-	
C_{rss}	Reverse transfer capacitance		-	64	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = 40\text{ V}$, $I_{\text{D}} = 23\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Gate charge test circuit")	-	60	-	nC
Q_{gs}	Gate-source charge		-	24.7	-	
Q_{gd}	Gate-drain charge		-	14.8	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 40\text{ V}$, $I_{\text{D}} = 11.5\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13: "Switching times test circuit for resistive load" and Figure 18: "Switching time waveform")	-	34.5	-	ns
t_{r}	Rise time		-	16.8	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	60	-	
t_{f}	Fall time		-	15.4	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{\text{SD}}^{(1)}$	Forward on voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{SD}} = 23\text{ A}$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{\text{SD}} = 23\text{ A}$, $\text{di/dt} = 100\text{ A}/\mu\text{s}$, $V_{\text{DD}} = 64\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	48.6		ns
Q_{rr}	Reverse recovery charge		-	65.6		nC
I_{RRM}	Reverse recovery current		-	2.7		A

Notes:

(1) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

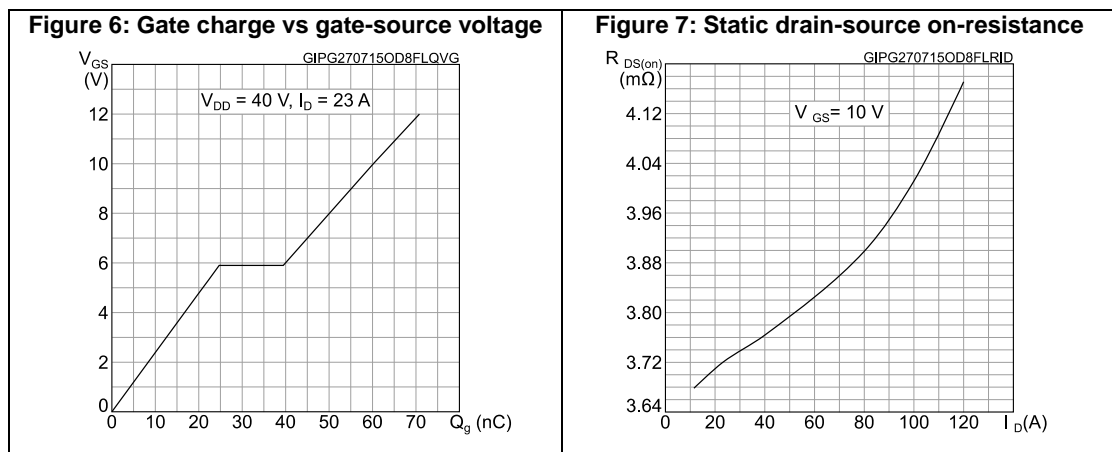
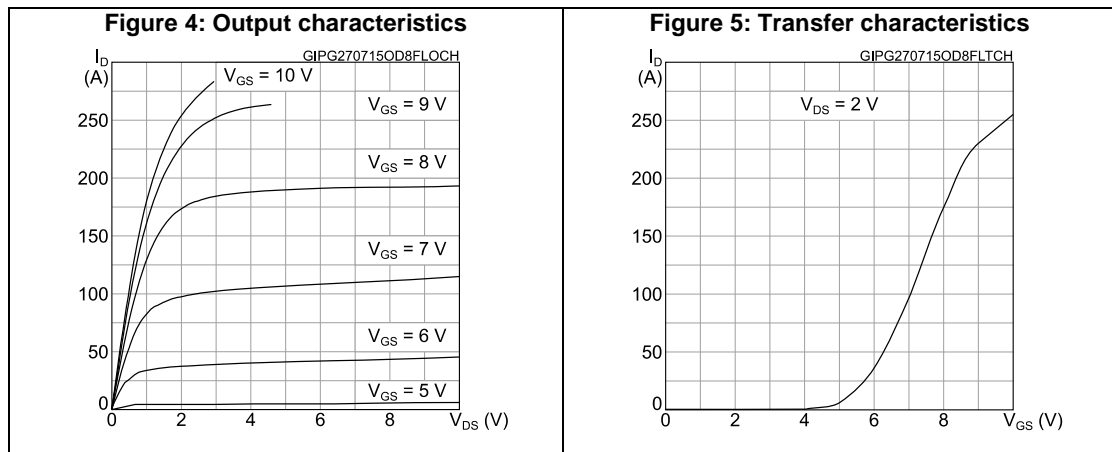
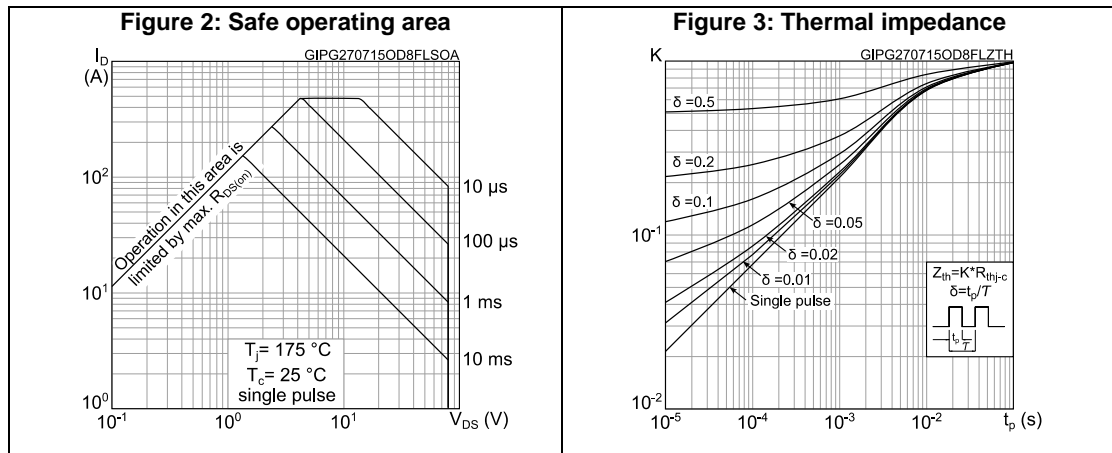


Figure 8: Capacitance variations

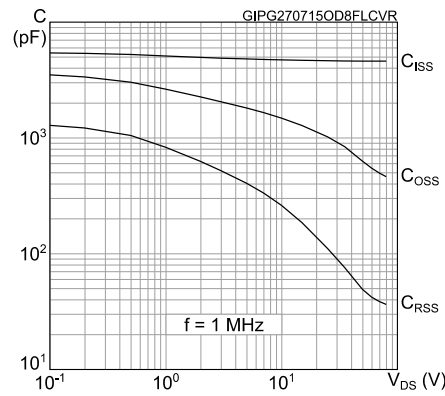


Figure 9: Normalized gate threshold voltage vs temperature

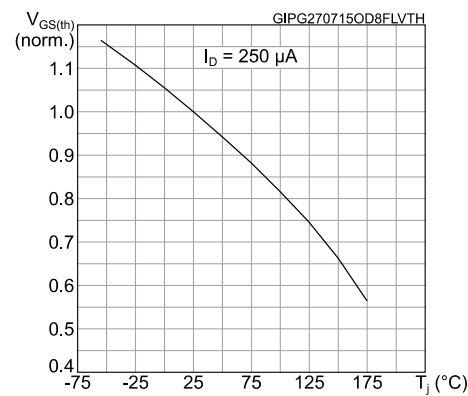


Figure 10: Normalized on-resistance vs temperature

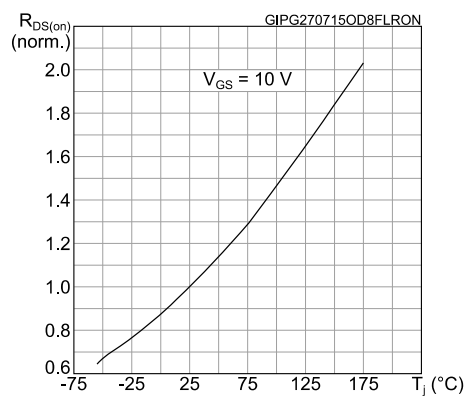


Figure 11: Normalized V(BR)DSS vs temperature

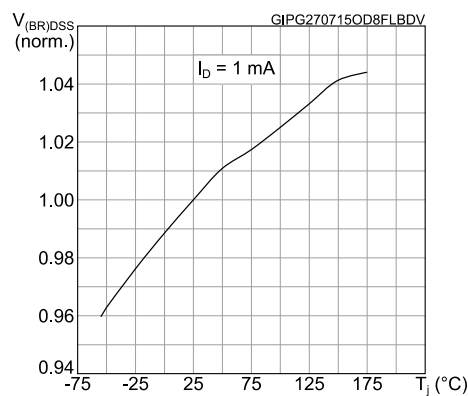
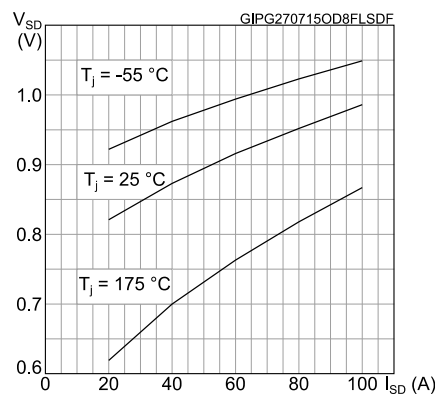
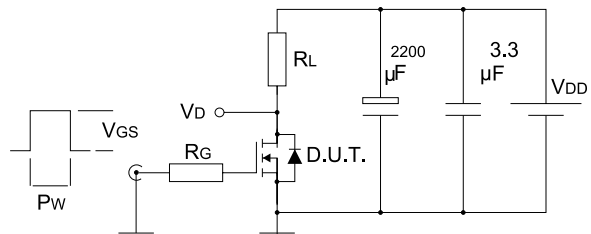


Figure 12: Source-drain diode forward characteristics



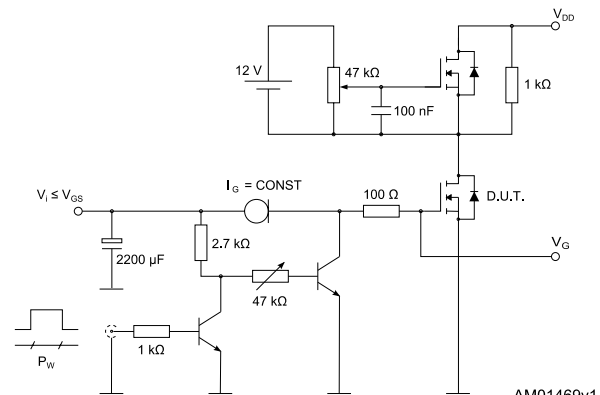
3 Test circuits

Figure 13: Switching times test circuit for resistive load



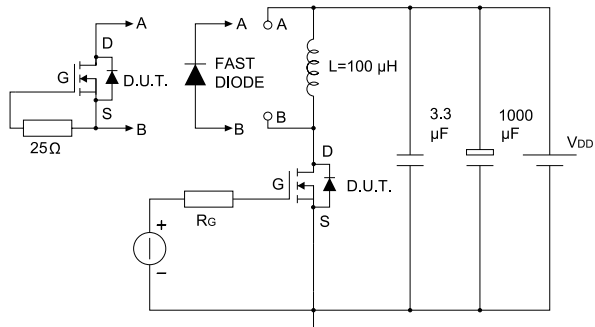
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Figure 14: Gate charge test circuit



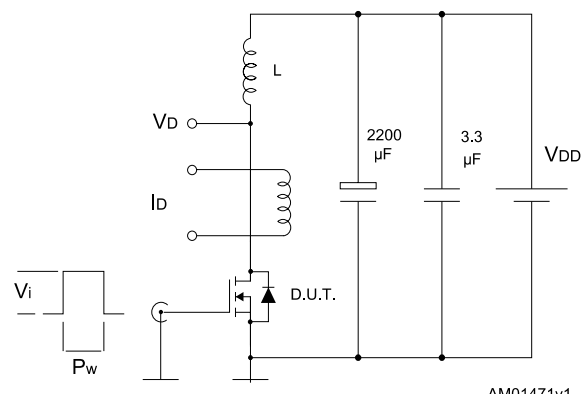
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Figure 15: Test circuit for inductive load switching and diode recovery times



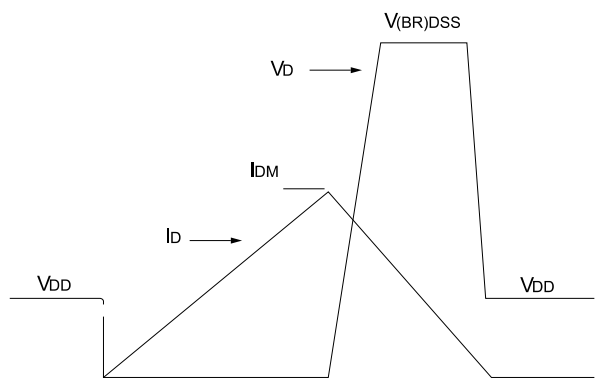
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Figure 16: Unclamped inductive load test circuit



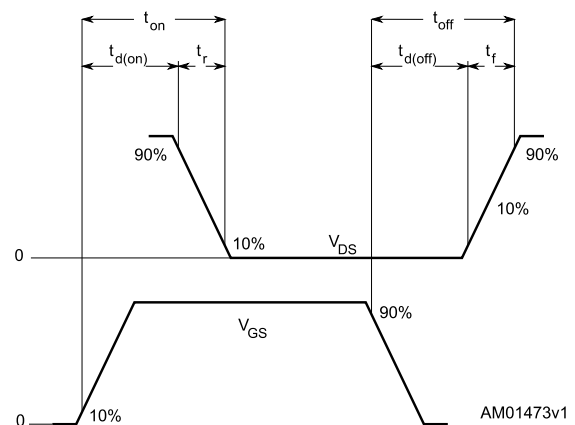
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 type C package

Figure 19: PowerFLAT™ 5x6 type C package outline

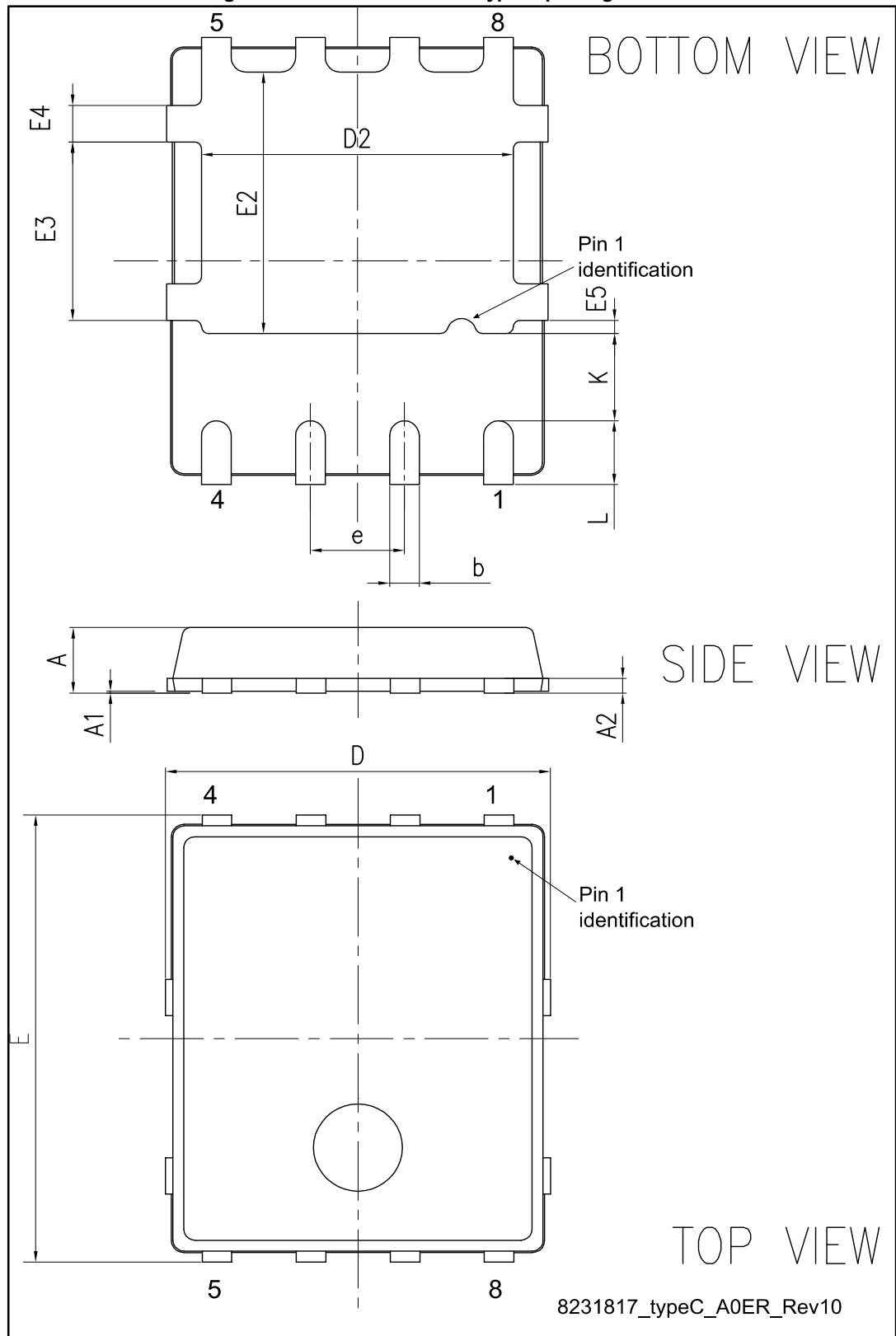
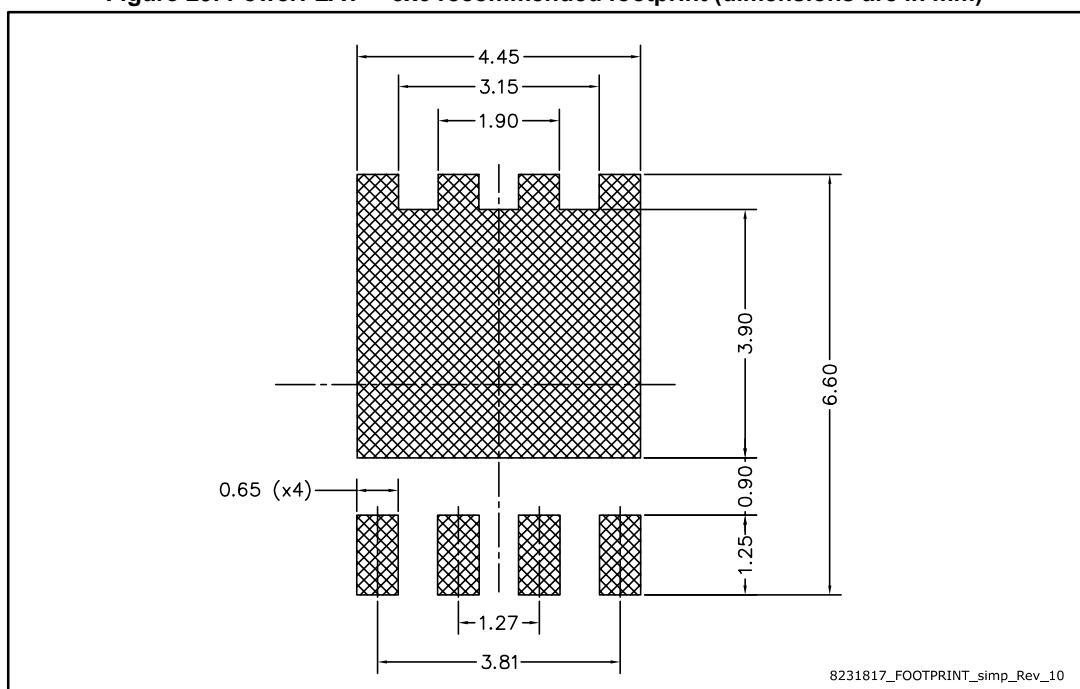


Table 8: PowerFLAT™ 5x6 type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

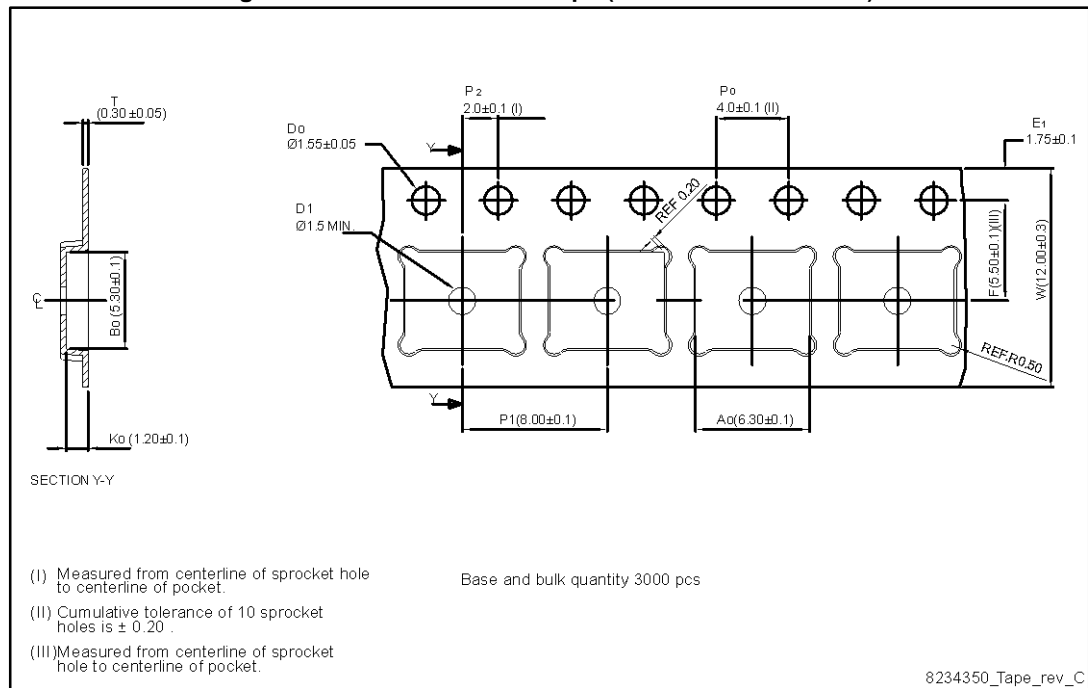
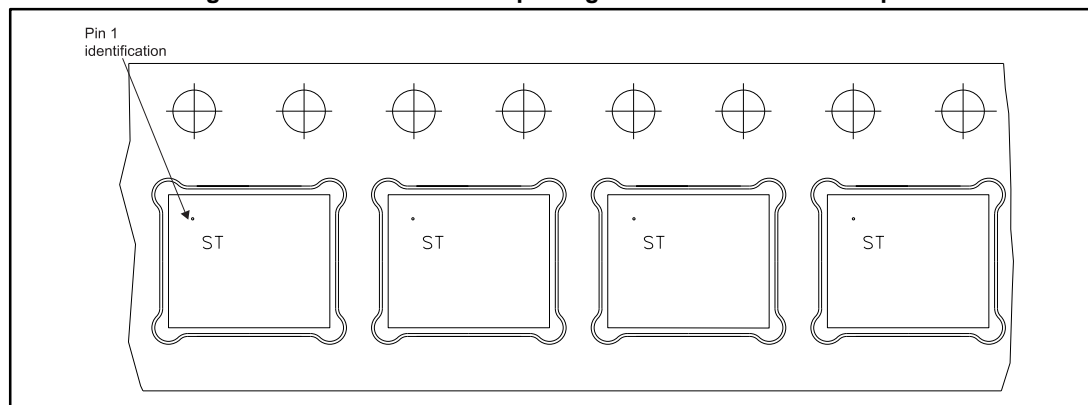


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape



Technical drawing of a reel tape showing front, side, and core details with dimensions in millimeters.

Front View (Left): Circular reel tape with a central hub. Dimensions include: PART NO. (top left), R25.00 (outer radius), 4.00 (inner radius), 2.50 (width of the central hole), and 128 (width of the tape).

Side View (Right): Shows the profile of the reel tape. Dimensions include: W3 11.9/15.4 (top width), W2 18.4 (max) (middle width), 2N 178(±2.0) (middle thickness), W1 12.4 (+2/-0) (bottom width), and A 330 (+0/-4.0) (total height).

Core Detail (Bottom Left): Detailed view of the central hub. Dimensions include: R1.10 (inner radius), Ø21.2 (inner diameter), Ø13.00 (outer diameter), and 2.20 (width of the hub).

ESD LOGO: A logo is present on the side view, indicating Electrostatic Discharge protection.

All dimensions are in millimeters

8234350 Reel rev

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
09-Dec-2014	1	First release.
27-Jul-2015	2	Text and formatting changes throughout document. Datasheet status promoted from preliminary data to production data. In section <i>Electrical characteristics</i> : - updated tables <i>Dynamic</i> , <i>Switching times</i> and <i>Source-drain diode</i> - added section <i>Electrical characteristics (curves)</i>

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