



PMZ130UNE

20 V, N-channel Trench MOSFET

12 March 2015

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006-3 (SOT883) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Very fast switching
- Low threshold voltage
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection: 2 kV HBM
- Leadless ultra small package: $1.0 \times 0.6 \times 0.48$ mm

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

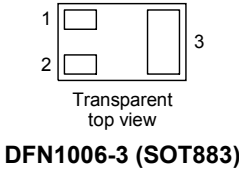
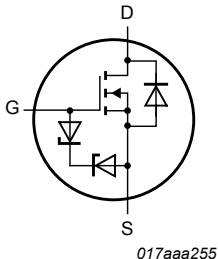
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_J = 25\text{ }^{\circ}\text{C}$		-	-	20	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-	1.8	A
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 1.8\text{ A}; T_J = 25\text{ }^{\circ}\text{C}$		-	120	150	m Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2 .



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DFN1006-3 (SOT883)	 017aaa255
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZ130UNE	DFN1006-3	DFN1006-3: leadless ultra small plastic package; 3 solder lands	SOT883

7. Marking

Table 4. Marking codes

Type number	Marking code
PMZ130UNE	ZU

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	20	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	1.8	A
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	1.2	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	8	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	350	mW
			[1]	-	760	mW
		T _{sp} = 25 °C		-	6250	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	0.7	A

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

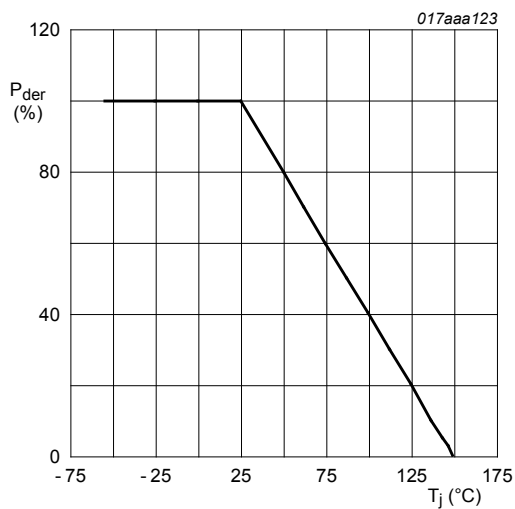


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$

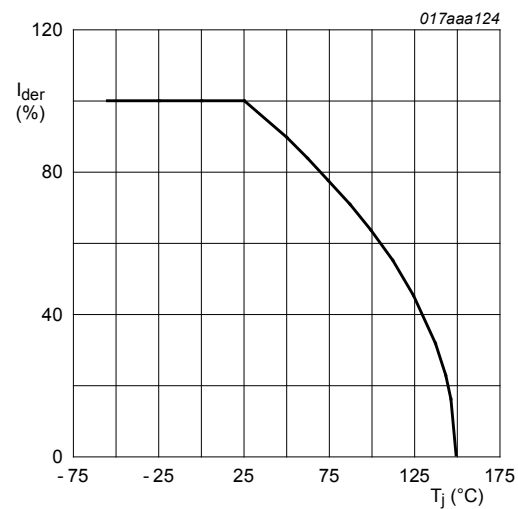
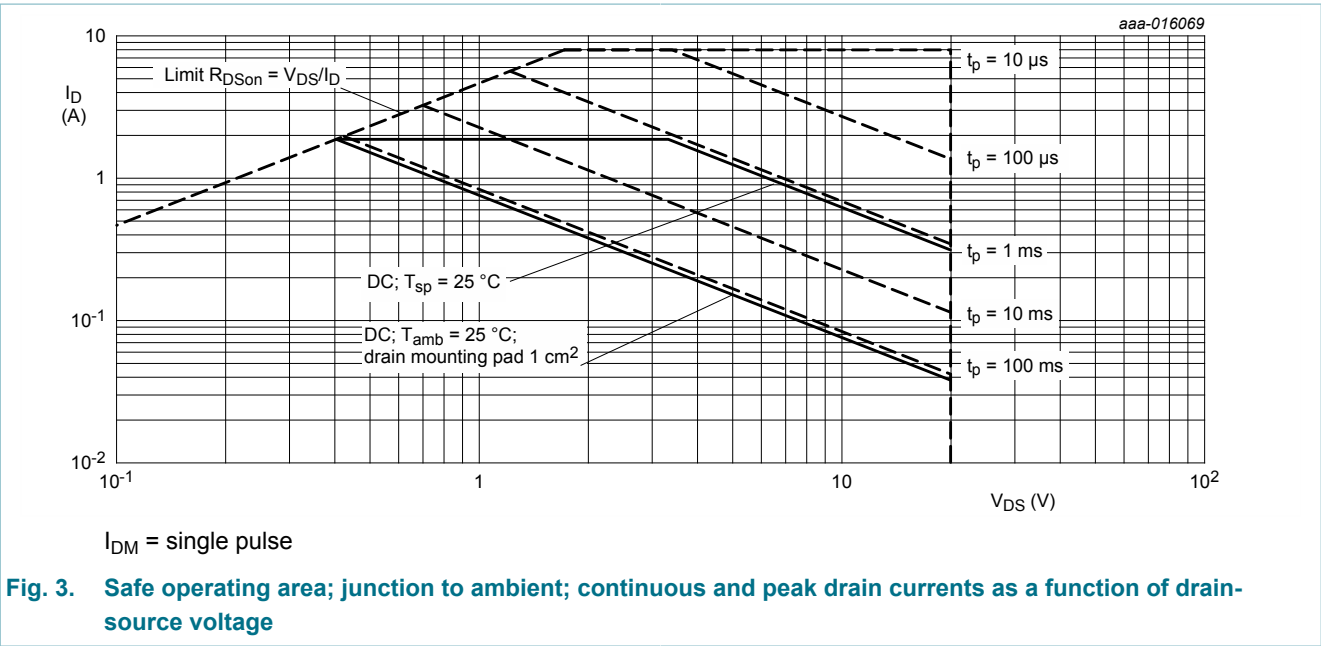


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

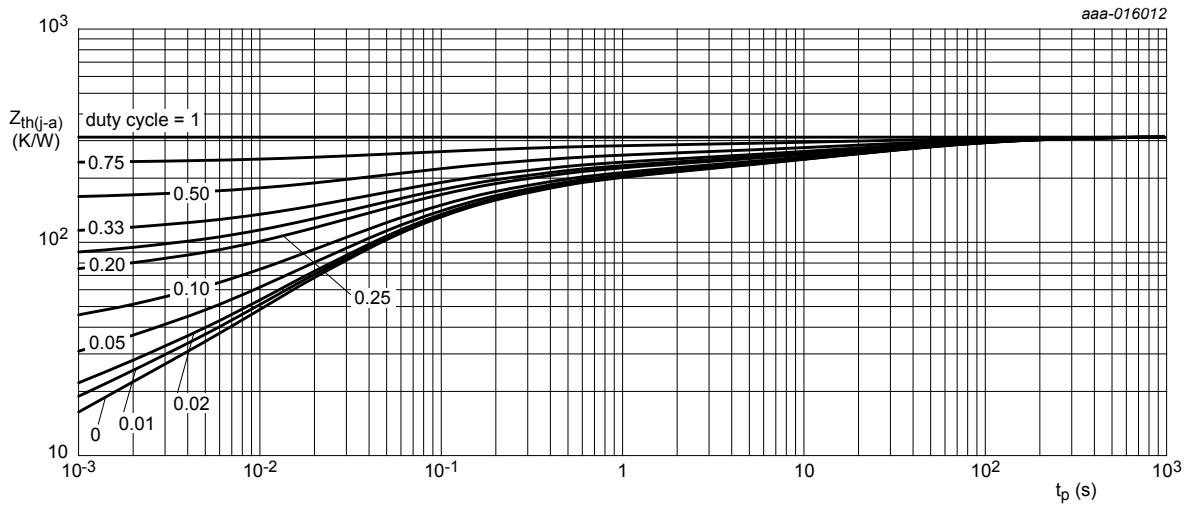


9. Thermal characteristics

Table 6. Thermal characteristics

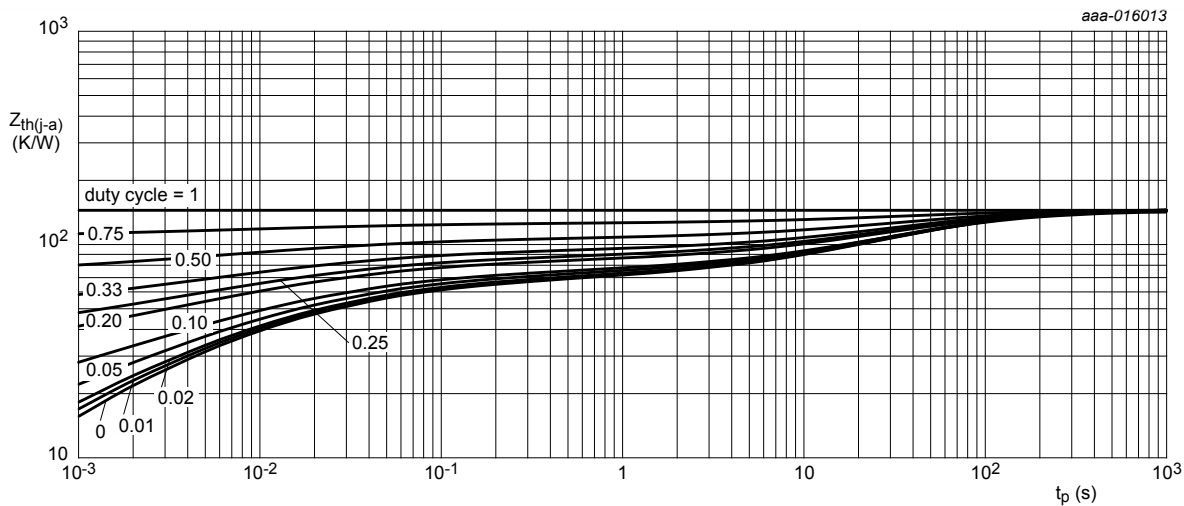
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	315	360	K/W
			[2]	-	145	165	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	17	20	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		20	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		0.45	0.7	0.95	V
I _{DSS}	drain leakage current	V _{DS} = 20 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
I _{GSS}	gate leakage current	V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C		-	-	5	μA
		V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-5	μA
		V _{GS} = 4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -4.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{GS} = 2.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
		V _{GS} = -2.5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 1.8 A; T _j = 25 °C		-	120	150	mΩ
		V _{GS} = 4.5 V; I _D = 1.8 A; T _j = 150 °C		-	178	220	mΩ
		V _{GS} = 2.5 V; I _D = 1.5 A; T _j = 25 °C		-	160	220	mΩ
		V _{GS} = 1.8 V; I _D = 0.25 A; T _j = 25 °C		-	210	310	mΩ
		V _{GS} = 1.5 V; I _D = 0.01 A; T _j = 25 °C		-	270	530	mΩ
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 1.6 A; T _j = 25 °C		-	4.1	-	S
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = 10 V; I _D = 1.6 A; V _{GS} = 4.5 V; T _j = 25 °C		-	1.6	-	nC
Q _{GS}	gate-source charge			-	0.15	-	nC
Q _{GD}	gate-drain charge			-	0.44	-	nC
C _{iss}	input capacitance	V _{DS} = 10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	93	-	pF
C _{oss}	output capacitance			-	18	-	pF
C _{rss}	reverse transfer capacitance			-	16	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 10 V; I _D = 1.6 A; V _{GS} = 4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	5.3	-	ns
t _r	rise time			-	12	-	ns
t _{d(off)}	turn-off delay time			-	16	-	ns
t _f	fall time			-	5	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 0.7 A; V _{GS} = 0 V; T _j = 25 °C		-	0.8	1.2	V

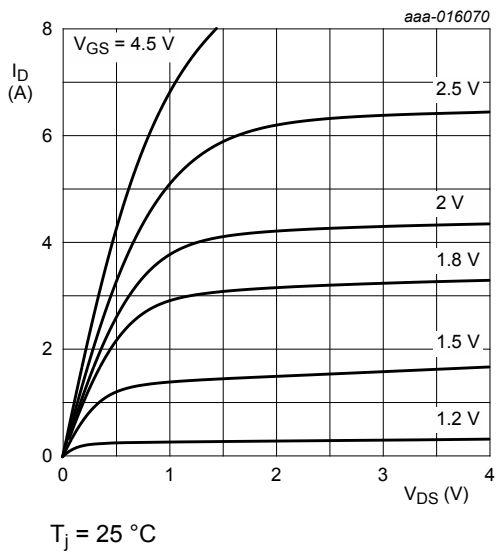


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

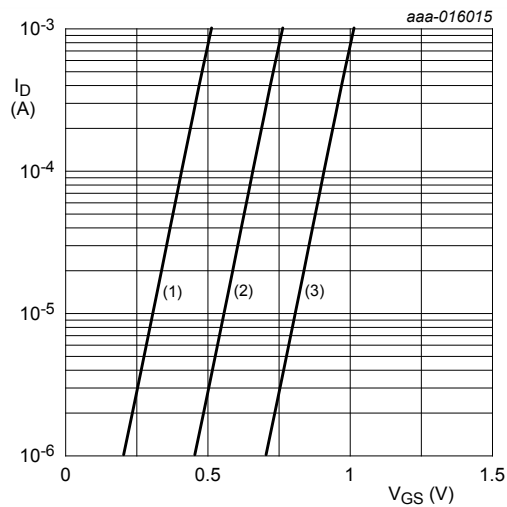


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

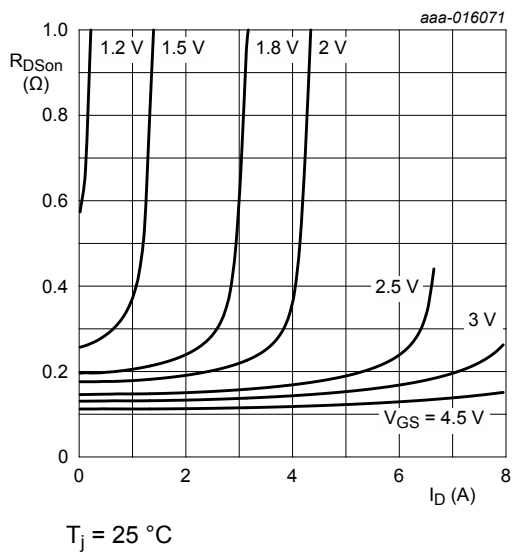


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

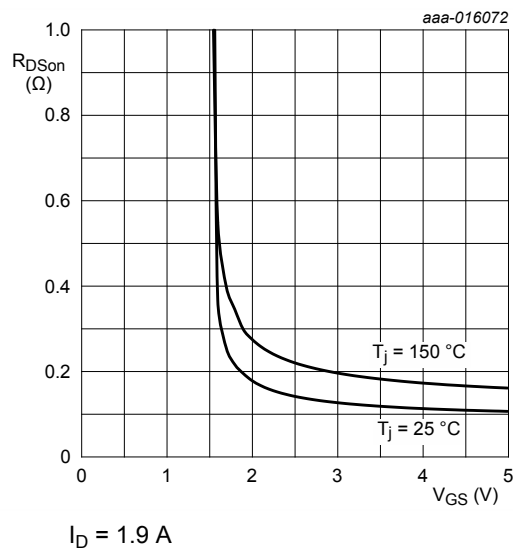
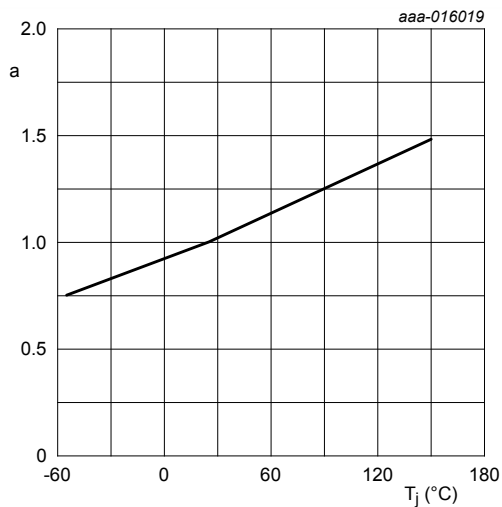
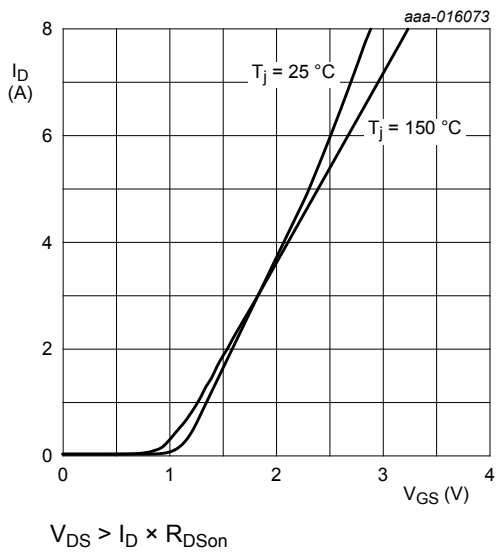
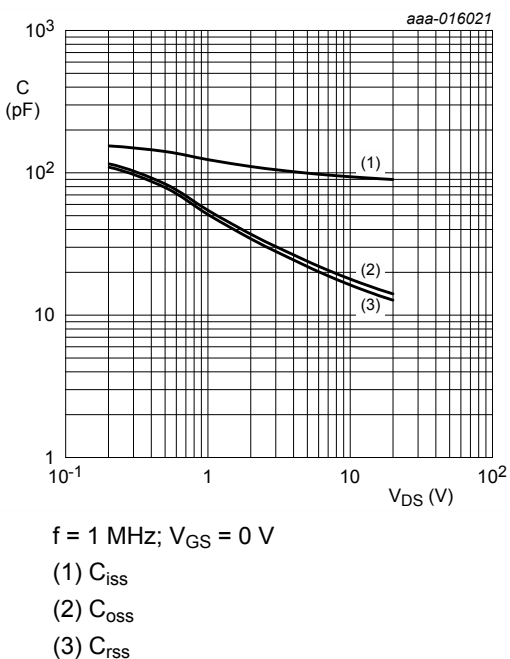
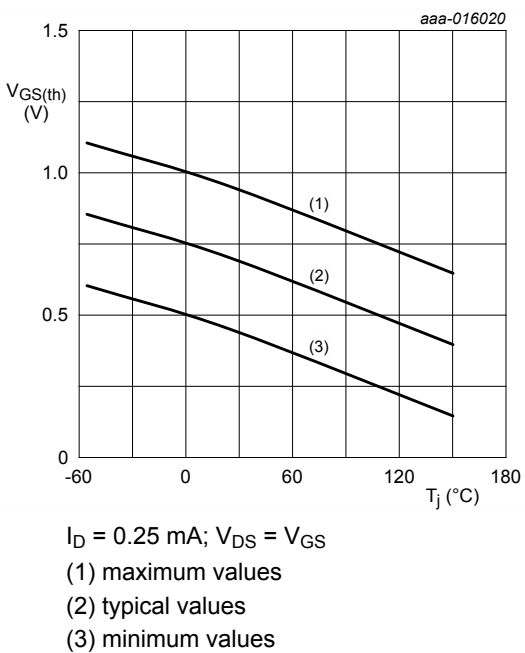


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$



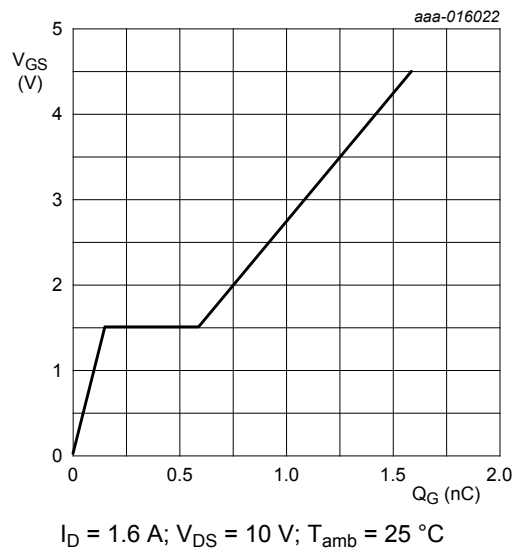


Fig. 14. Gate-source voltage as a function of gate charge; typical values

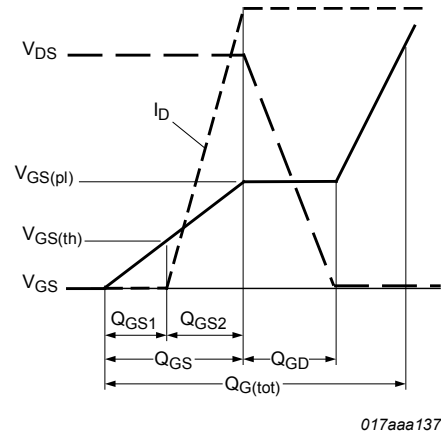


Fig. 15. MOSFET transistor: Gate charge waveform definitions

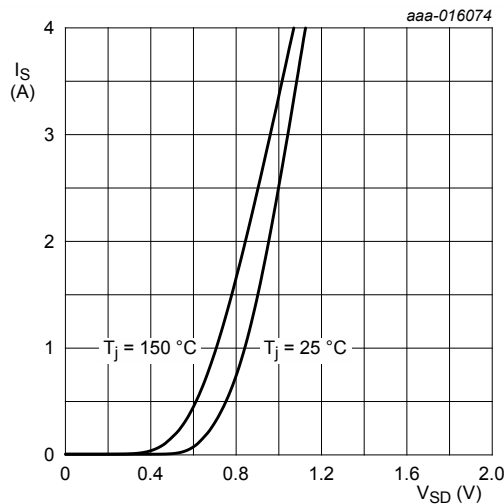


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

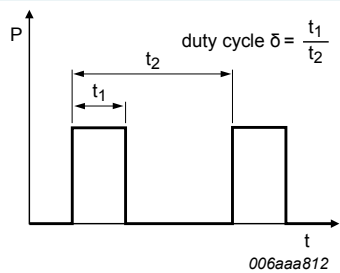
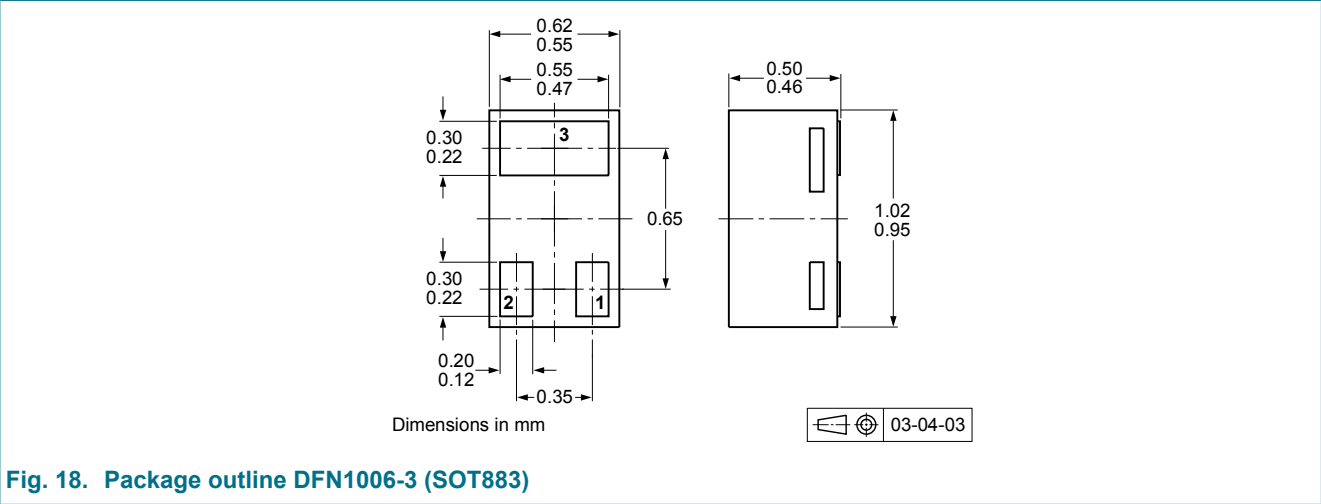
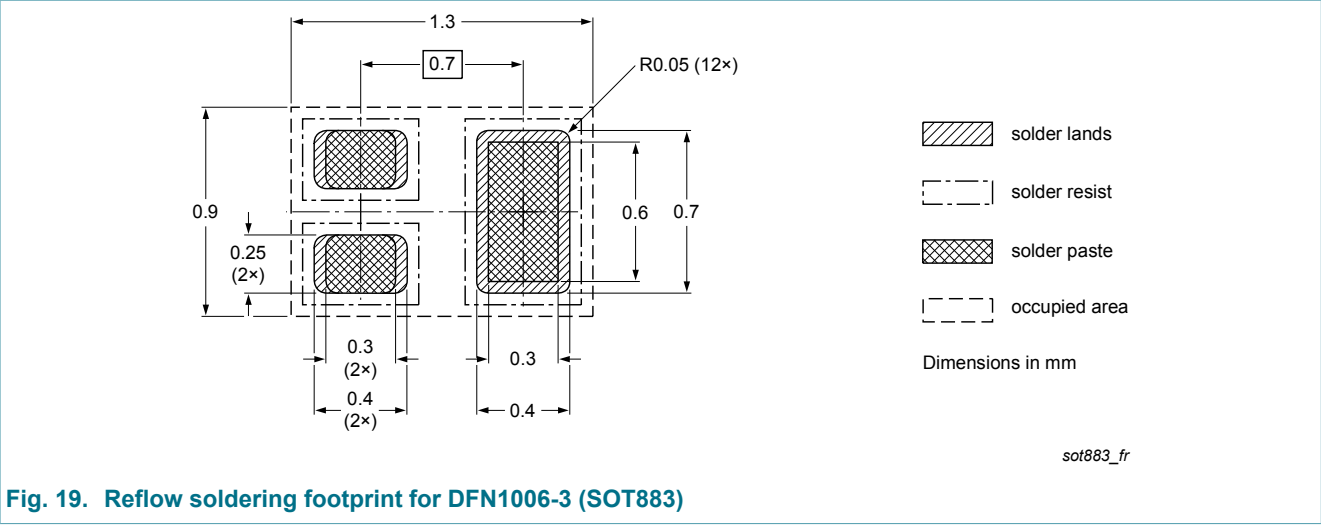


Fig. 17. Duty cycle definition

12. Package outline



13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMZ130UNE v.1	20150312	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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