# OPA521 Narrowband Power Line Communications Line Driver

## 1 Features

- Supports:
  - CENELEC Bands A, B, C, D
  - ARIB STD-T84, FCC
  - FSK, SFSK, and NB-OFDM
- Conforms To:
  - EN50065-1, -2, -3, -7
  - FCC, Part 15
  - ARIB STD-T84
- Standards:
  - G3, PRIME, P1901.2, ITU-G.hnem
- Integrated Power-Line Driver With Thermal and Overcurrent Protection
- Pin-Selectable Quiescent Current Consumption:
  - 40 µA in Standby Mode (Typical)
  - 51 mA for CENELEC Bands A, B, C, D (Typical)
  - 78 mA for FCC, ARIB STD-T84, FCC (Typical)
- Package: 5 mm × 5 mm 20-Pin VQFN
- Extended Operating Temperature Range: $T_A$ = –40°C to +125°C

## 2 Applications

- eMetering
- Home Area Networks
- Lighting Applications
- Solar Applications
- Pilot Wires and EVSEs

## 3 Description

The OPA521 is a power line communications (PLC) line driver that meets the conducted emissions requirements in CENELEC bands A, B, C and D and ARIB STD-T84 and FCC Part 15. This device is designed for driving high-current, low-impedance lines up to 1.9 A into reactive loads. With optimized internal protection structures, the OPA521 requires minimal external protection components that enable a minimal system solution cost.

The OPA521 gives a closed-loop gain of 7 with a 3.8-MHz bandwidth. The monolithic integrated circuit gives high reliability in power line communication applications.

The OPA521 transmit power amplifier operates from a single supply from 7 V to 24 V. At a typical load current ($I_{OUT}$ = 1.9 $A_{PEAK}$), a wide output swing gives a 10-$V_{PP}$ capability with a nominal 24-V supply.

The device is internally protected against overtemperature and short-circuit conditions. Fault detection flags indicate current and thermal limits. A shutdown pin is available, and places the device into a low-power state, consuming 40 µA (typical).

The OPA521 is available in a surface-mount, 5 mm × 5 mm QFN, 20-pin package (RGW). Operation is specified over the extended industrial junction temperature range of –40°C to +125°C.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA521 | VQFN (20) | 5.00 mm × 5.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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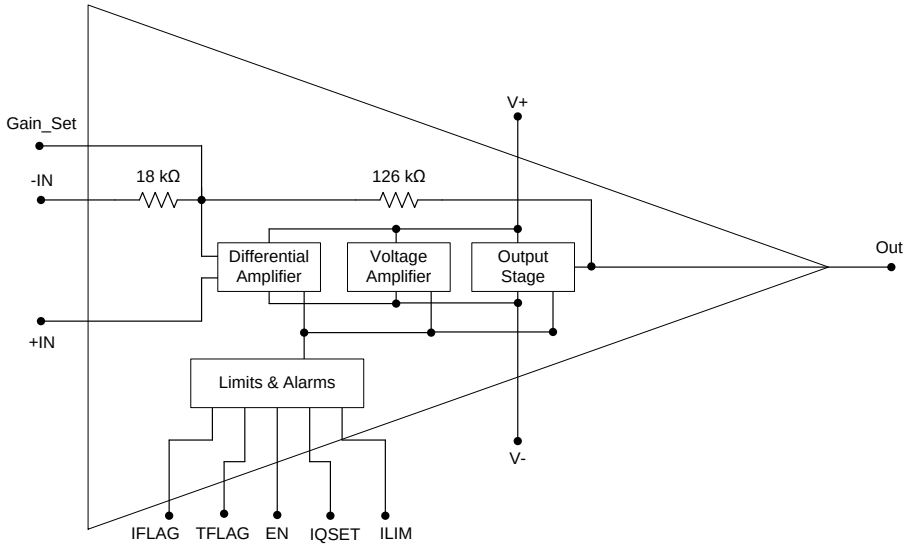

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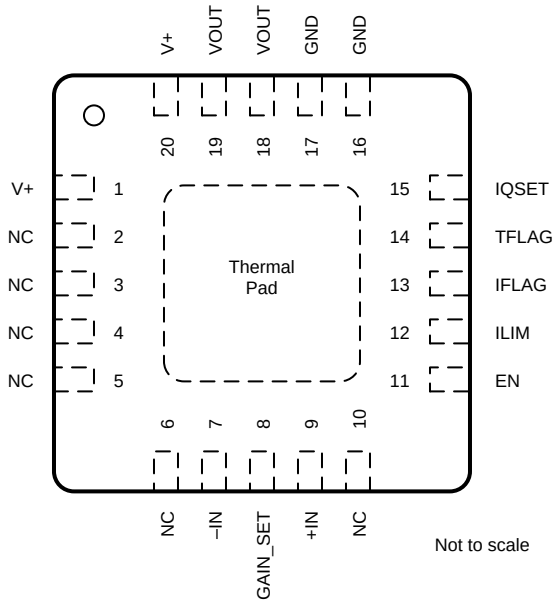
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| May 2018 | * | Initial release |

# 5 Pin Configuration and Functions

**RGW Package**
**20-Pin VQFN With Exposed Thermal Pad**
**Top View**




NC - no internal connection

**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 11 | I | Enables the amplifier (active high, high enables the OPA521) |
| GAIN_SET | 8 | I | Connect an external resistor to Gain_Set and -IN to increase the gain above -7 V/V |
| GND | 16, 17 | — | Ground |
| IFLAG | 13 | O | Current limit warning flag (open-drain, active high, high signifies current limit condition) |
| ILIM | 12 | I | Resistor programmable current limit |
| +IN | 9 | I | Non-inverting input (connect to a voltage equal to (V+)/2) |
| –IN | 7 | I | Inverting input for closed loop gain = –7 V/V |
| IQSET | 15 | I | Quiescent current select (active high, high configures the OPA521 to operate in FCC/ARIB bands, low configures the OPA521 to operate in CENELEC Bands A, B, C, D) |
| NC | 2, 3, 4, 5, 6, 10 | — | No internal connection |
| TFLAG | 14 | O | Thermal limit warning flag (open-drain, active high, high signifies thermal limit condition) |
| V+ | 1, 20 | — | Positive power supply |
| VOUT | 18. 19 | O | Output |
| Thermal pad | | — | Must be soldered to PCB and connected to GND |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, V+ | | Pins 1, 20 | GND + 26 | | V |
| Signal input terminals | Voltage | Pins 7, 8, 9, 12 | GND – 0.4 | V+ + 0.4 | V |
| | | Pins 11, 15 | GND – 0.4 | 5.5 | |
| | Current | Pins 7, 8, 9, 11, 12, 15 | | ±10 | mA |
| Signal output terminals | Voltage | Pins 18, 19 | GND – 0.4 | V+ + 0.4 | V |
| | | Pins 13, 14 | GND – 0.4 | 5.5 | |
| | Current; short-circuit to GND | Pins 13, 14, 18, 19 | Continuous | | |
| Operating temperature, $T_A$ | | | –40 | 150 | °C |
| Operating junction temperature, $T_J$ | | | –55 | 150 | °C |
| Storage temperature, $T_{stg}$ | | | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±3000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Thermal Information

| THERMAL METRIC(1) | | OPA521 RGW (QFN) 20 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 33.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 30.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 12.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 12.5 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.4 Electrical Characteristics

at $T_{CASE}$ = 25°C, V+ = 15 V, IN+ = (V+) / 2, $R_{LOAD}$ 50 Ω, (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **NOISE** | | | | | |

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## Electrical Characteristics (continued)

at $T_{CASE}$ = 25°C, V+ = 15 V, IN+ = (V+) / 2, $R_{LOAD}$ 50 Ω, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Integrated output noise | CEN-A, 35 kHz to 95 kHz | | 370 | | $\mu V_{RMS}$ |
| | | CEN-B, 95 kHz to 125 kHz | | 220 | | $\mu V_{RMS}$ |
| | | CEN-C, 125 kHz to 140 kHz | | 160 | | $\mu V_{RMS}$ |
| | | CEN-D, 140 kHz to 148 kHz | | 98 | | $\mu V_{RMS}$ |
| | | ARIB STD-T84, 35 kHz to 420 kHz | | 640 | | $\mu V_{RMS}$ |
| | | FCC-LOW, 35 kHz to 125 kHz | | 384 | | $\mu V_{RMS}$ |
| | | G3-FCC, 150 kHz to 490 kHz | | 565 | | $\mu V_{RMS}$ |
| **INPUT** | | | | | | |
| | Input voltage range | For linear operation | (GND + 0 / 4) | | ((V+) – 0.4 / 7) | V |
| | Input impedance | | | 18 | | kΩ |
| **FREQUENCY RESPONSE** | | | | | | |
| BW | Bandwidth | $I_{LOAD}$ = 0 mA | 3.4 | 3.82 | 4.23 | MHz |
| SR | Slew rate | V+ = 24 V, $V_{OUT}$ = 20-V step, $I_{LOAD}$ = 0 mA | | 75 | | V/µs |
| | Full-power bandwidth | V+ = 24 V, $V_{OUT}$ = 20 $V_{PP}$ | | 1 | | MHz |
| PSRR | Power-supply rejection ratio | RTI, DC to f = 50 kHz | 80 | 94 | | dB |
| **OUTPUT** | | | | | | |
| $V_O$ | Voltage output swing | From V+, $I_O$ = 200-mA sourcing, 1-ms pulse | | | 0.5 | V |
| | | From V+, $I_O$ = 1.5-A sourcing, 1-ms pulse | | | 2.25 | V |
| | From GND | From GND, $I_O$ = 200 mA sinking, 1-ms pulse | | | 0.5 | V |
| | | From GND, $I_O$ = 1.5-A sinking, 1-ms pulse | | | 1.5 | V |
| | Maximum continuous current, DC | Pin 8 connected to ground | | 1.9 | | A |
| | Output resistance | $I_O$ = 1.9 A, f = 500 kHz | | 0.1 | | Ω |
| | Disabled output impedance | f = 100 kHz | | 130 \|\| 105 | | kΩ \|\| pF |
| | Output current limit | Resistor selectable, $R_{SET}$ connected from pin 6 to ground | | 2.5 | | A |
| **GAIN** | | | | | | |
| G | Nominal gain | $V_{OUT}/V_{IN}$ | | –7 | | V/V |
| $G_E$ | Gain error | $T_J$ = –40°C to +125°C | –2% | 0.1% | 2% | |
| | Gain error drift | $T_J$ = –40°C to +125°C | | ±5 | | ppm/°C |
| **THERMAL SHUTDOWN** | | | | | | |
| | Junction temperature at shutdown | | | 165 | | °C |
| | Hysteresis | | | 15 | | °C |
| | Return to normal operation | | | 150 | | °C |

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## 6.5 Electrical Characteristics: Digital

at $T_{CASE}$ = +25°C, V+ = 15 V, IN+ = (V+) / 2, $R_{LOAD}$ 50 Ω, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS (ENABLE, IQSET)** | | | | | | |
| | Leakage input current | (V-) ≤ $V_{IN}$ ≤ 5.5 | –1 | 0.01 | 1 | µA |
| $V_{IH}$ | High-level input voltage | | (V–) + 2 | (V–) + 2 | 5.5 | V |
| $V_{IL}$ | Low-level input voltage | | V- | | (V–) + 0.8 | V |
| | EN pin function (active high) | EN pin high, EN > (V–) + 2 | Device in normal operation | | | |
| | | EN pin low, EN < (V–) + 0.8 | Device in shutdown | | | |
| | IQSET pin function (active high) | IQSET pin high, IQSET > (V–) + 2 | Device in FCC or ARIB mode (Iq = 78 mA [typical]) | | | |
| | | IQSET pin low, IQSET < (V–) + 0.8 | Device in CENELEC mode (Iq = 48 mA [typical]) | | | |
| **DIGITAL OUTPUTS (TFLAG, IFLAG)** | | | | | | |
| $I_{OH}$ | High-level output current | $V_{OH}$ = 3.3 V | | | 1 | µA |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA | | | 0.4 | V |
| $I_{OL}$ | Low-level output current | $V_{OL}$ = 400 mV | 4 | | | mA |

## Electrical Characteristics: Digital (continued)

at $T_{CASE}$ = +25°C, V+ = 15 V, IN+ = (V+) / 2, $R_{LOAD}$ 50 Ω, (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| TFLAG (active high, open-drain) | TFLAG pin high, TFLAG sink high < 1 µA | Device is in thermal shutdown | | | |
| | TFLAG pin low, TFLAG < 0.4 V | Device is not in thermal shutdown | | | |
| IFLAG (active high, open-drain) | IFLAG pin high, IFLAG sink high < 1 µA | Device is in current limit | | | |
| | IFLAG pin low, IFLAG < 0.4 V | Device is not in current limit | | | |
| **SHUTDOWN MODE TIMING** | | | | | |
| Enable time | SD pin transitions from low to high | | 3 | | ms |
| Disable time | SD pin transitions from high to low | | 2 | | ms |

## 6.6 Electrical Characteristics: Power Supply

at $T_{CASE}$ = 25°C, V+ = 15 V, IN+ = (V+) / 2, $R_{LOAD}$ 50 Ω, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPERATING SUPPLY RANGE** | | | | | | |
| V+ | Power amplifier | | 7 | 15 | 24 | V |
| **QUIESCENT CURRENT (ENABLE PIN HIGH)** | | | | | | |
| IQ | FCC or ARIB mode | $I_O$ = 0 A, IQSET pin high | 68 | 78 | 88 | mA |
| | CENELEC mode | $I_O$ = 0 A, IQSET pin low | 38 | 48 | 58 | mA |
| **SHUTDOWN (ENABLE PIN LOW)** | | | | | | |
| EN | Power amplifier | EN pin low | | 40 | 150 | µA |

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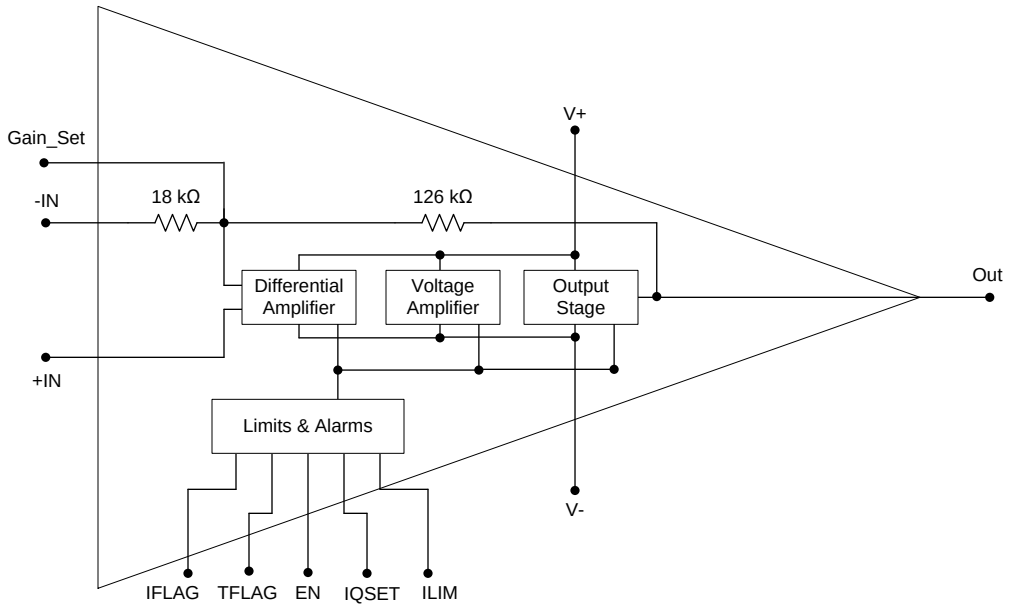
# 7 Detailed Description

## 7.1 Overview

The OPA521 is a power amplifier designed for power line communication (PLC) applications. The device features a fixed gain of –7 V/V, low-pass filter response, excellent linearity and low distortion through the bandwidth. The amplifier operates with 7-V to 24-V supplies, and can deliver up to ±1.9 A of continuous current from –40°C to +125°C.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

The OPA521 offers an optional output current limit (ILIM), quiescent current (IQSET) selection pins, and a device enable pin. The IFLAG output alarm pin indicates an output current warning and the TFLAG alarm triggers when the internal temperature of the device forces the devices to shut down.

## 7.4 IQSET Pin

This pin sets the operating band of the amplifier by adjusting the quiescent current.

- IQSET > 2 V sets the device to operate in the FCC or ARIB bands
- IQSET < 0.8 V sets the device to operate in the CENELEC bands

## 7.5 EN Pin

When the transmitter is not in use, the output is disabled and placed in a high-impedance state when the EN pin decreases. For typical operation, connect the EN pin to 3.3 V. In disabled mode, the entire device draws 40 μA (typical) of current.

## 7.6 ILIM Pin Current Limiting

The ILIM pin (pin 12) provides a resistor-programmable output current limit. Equation 1 determines the value of the external $R_{SET}$ resistor attached to this pin.

$$I_{LIM} = \frac{1.2\ V \times 16.320\ k\Omega}{8\ k\Omega + R_{SET}}$$

where:

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### ILIM Pin Current Limiting (continued)

- $R_{SET}$ = the value of the external resistor connected between pin 26 and ground,
- and
- $I_{lim}$ = the value of the desired current limit. (1)

There is a 30% tolerance on the $I_{lim}$ value given by Equation 1.

## 7.7 IFLAG and TFLAG Pins

The IFLAG and TFLAG pins are active-high, open-drain outputs that indicate if the OPA521 is in current or thermal limit. Connect these pins to 3.3 V through pullup resistors (for example 10 kΩ).

The maximum output current from the power amplifier is programmed with the external $I_{LIM}$ resistor that is connected between ILIM (pin 12) and ground. IFLAG is set if the amplifier goes to a current limit state if a fault condition occurs. This causes the PA to source or sink more current than the programmed limit value. IFLAG exhibits transient pulses under typical operation. An IFLAG true state for greater than 100 ms is a definite indication of a fault current condition.

The device contains internal thermal shutdown protection circuitry that automatically disables the output stage if the junction temperature exceeds 165°C. The device thermal shutdown protection circuitry lets the amplifier typical normal operation only when the junction temperature falls below 150°C. The TFLAG is active when the device is in thermal shut down mode.

## 7.8 Device Functional Modes

The OPA521 operates from a single power rail from 7 V to 24 V. The gain is set at –7 V/V and can increase with an external resistor that is connected to the GAIN_SET and –IN pins.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The OPA521 is an integrated, power line communication power amplifier that transmits PLC data onto power lines through a line-coupling circuit.

## 8.2 Typical Application

A schematic for a typical application is provided in Figure 1.

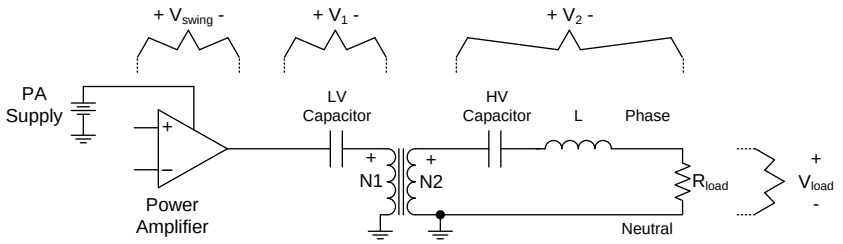


**Figure 1. Typical Line Coupling Circuit**

### 8.2.1 Design Requirements

For typical power line applications, use the following parameters:

**Table 1. Power-Supply Requirements**

| PARAMETER | FSK OR SFSK | PRIME OR G3 OFDM | UNITS |
|---|---|---|---|
| Frequency range | 63 to 74 | 35 to 95 | kHz |
| $R_{LOAD}$ | 2 | 2 | Ω |
| $V_{LOAD}$ | 1 | 1 | $V_{RMS}$ |
| $V_{LOAD}$ | 1.414 | 3 | $V_{PEAK}$ |
| $V_{LOAD}$ | 2.828 | 6 | $V_{PP}$ |
| OFDM multiplier | — | 1.5 | — |
| $V_{SWING}$ | 2 | 2 | V |
| Turns ration, N1/N2 | 1.5 | 1.5 | — |
| PA supply | 8.25 | 17.5 | V |

**Example:**

For PRIME or G3 using an OFDM signal with a 2-Ω load and 1-$V_{RMS}$load voltage:

$PA_{Supply}$= $V_{LOAD}$ × OFDM Multiplier × Turns Ration + (2 × $V_{SWING}$)

$PA_{Supply}$= 6 V × 1.5 × 1.5 + (2 × 2 V)

$PA_{Supply}$= 17.5 V

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### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 System Examples*

##### 8.2.2.1.1 Power Amplifier Block

This power amplifier transmits data onto power lines through a line-coupling circuit. The power amplifier consists of a high slew rate, high-voltage, and high-current operational amplifier. The amplifier is configured with an inverting gain of 7 V/V and maintains excellent linearity and low distortion throughout the bandwidth. The amplifier operates from 7 V to 24 V and can deliver up to ±1.9 A of continuous output current over the specified junction temperature range of –40°C to +125°C. Connecting the amplifier in a typical power line communication (PLC) application requires a few additional components. Figure 2 shows the typical connections to the amplifier.

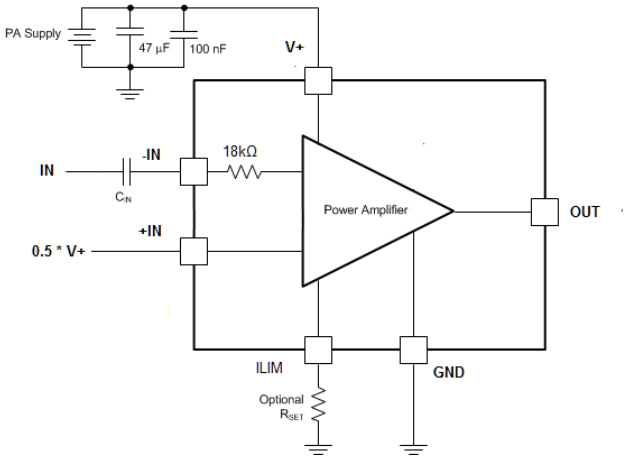


**Figure 2. Typical Connections to the Amplifier**

###### *8.2.2.1.1.1 +IN Connection*

The +IN pin provides the correct half power supply bias for the quiescent output voltage. The +IN pin is always connected to a DC bias equal to (V+) / 2.

###### *8.2.2.1.1.2 -IN Connection*

The external capacitor ($C_{IN}$) introduces a single-pole, high-pass characteristic to the transfer function. The $C_{IN}$ and amplifier combination has a band-pass response because of the inherent low-pass transfer function from the amplifier. The value of the high-pass cutoff frequency is determined by $C_{IN}$ that reacts with the input resistance of the amplifier circuit. Equation 2 calculates this value:

$$C_{IN} = \frac{1}{2 \times \pi \times 18\ k\Omega \times f_{HP}} \quad (2)$$

where:

- $C_{IN}$ = external input capacitor and
- $f_{HP}$ = desired high-pass cutoff frequency.

For example, setting $C_{IN}$ to 3.3 nF results in a high-pass cutoff frequency of 2.9 kHz. The voltage rating for $C_{IN}$ must be determined to withstand operation up to the PA power supply voltage.

$C_{IN}$ sets a DC gain of unity. This biases the DC output of the amplifier to the same level that is applied to the +IN, which must always be connected to a noise-free, low-impedance source of one-half of the supply voltage (V+).

#### *8.2.2.2 Line-Coupling Circuit*

The line-coupling circuit is one of the most critical circuits in a power line modem. The line-coupling circuit blocks the low-frequency signal of the mains (commonly 50 Hz or 60 Hz) from damaging the low-voltage modem circuitry and couples the modem signal to and from the AC mains. Figure 3 shows a typical line-coupling circuit.

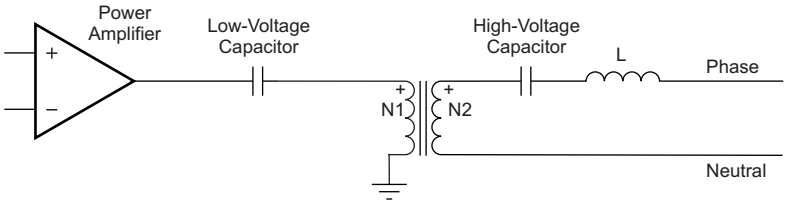




**Figure 3. Simplified Line-Coupling Circuit**

### *8.2.2.3 Circuit Protection*

Power-line communications are often located in operating environments that are harsh for electrical components connected to the AC line. Noise or surges from electrical anomalies (such as lightning, capacitor bank switching, inductive switching, or other grid fault conditions) can damage high-performance integrated circuits if proper protection is not provided. The power amplifier can survive the harshest conditions by using a variety of techniques to protect the device.

Lay out the protection circuitry to dissipate as much of the electrical disturbance as possible with a multilayer approach using metal-oxide varistors (MOVs), transient voltage suppression diodes (TVSs), Schottky diodes, and a Zener diode. These components dissipate the electrical disturbance before the anomaly reaches the device. Figure 4 shows the recommended strategy for transient overvoltage protection.

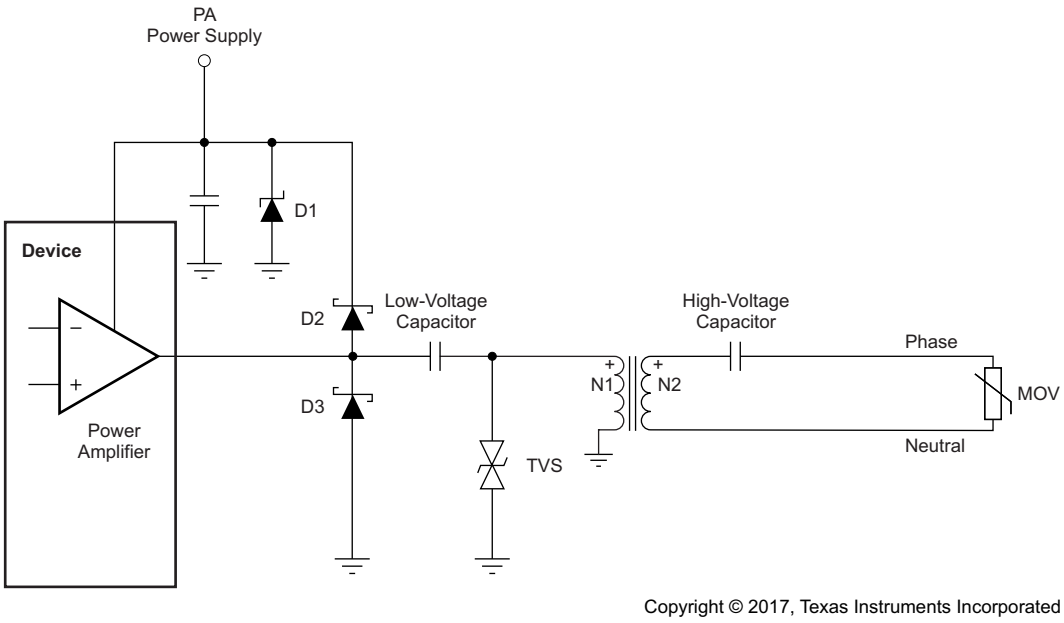




**Figure 4. Transient Overvoltage Protection**

The high-voltage coupling capacitor must be able to withstand pulses up to the clamping protection that are provided by the MOV. A metalized polypropylene capacitor (such as the 474MKP275KA from Illinois Capacitor™) is rated for 50 Hz to 60 Hz and 250 VAC to 310 VAC, and withstands 24 impulses of 2.5 kV.

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Table 2 and Table 3 list several recommended transient protection components.

**Table 2. Recommended Transient Protection Devices (120 VAC, 60 Hz)**

| COMPONENT | DESCRIPTION | MANUFACTURER | MFR PART NO. (OR EQUIVALENT) |
|---|---|---|---|
| D1 | Zener diode | TBD | TBD (1) |
| D2, D3 | Schottky diode | TBD | B340A |
| TVS | Transient voltage suppressor | TBD | TBD (2) |
| MOV | Varistor | Littelfuse, Inc. | TMOV20RP140E |
| HV capacitor | High-voltage capacitor | Illinois Capacitor, Inc | TBD (3) |

(1) Select the Zener breakdown voltage at the lowest available rating beyond the normal power supply operating range. For example, 1SMB5931B is designed for systems where PA_VS = 15 V, whereas 1SMB5934B is designed for systems where PA_VS = 20 V.
(2) Select the TVS breakdown voltage at or slightly less than (0.5 × PA_VS). For example, SMCJ6.0CA is designed for systems where PA_VS = 15 V, whereas SMCJ8.0CA is designed for systems where PA_VS = 20 V.
(3) A common value for the high-voltage capacitor is 470 nF. Other values may be substituted depending on the application requirements. When making a substitution, the capacitor must be selected from the same family or an equivalent family of capacitors rated to withstand high-voltage surges on the power line for reliability.

**Table 3. Recommended Transient Protection Devices (240 VAC, 50 Hz)**

| COMPONENT | DESCRIPTION | MANUFACTURER | MFR PART NO (OR EQUIVALENT) |
|---|---|---|---|
| D1 | Zener diode | TBD. | TBD (1) |
| D2, D3 | Schottky diode | TBD | TBD |
| TVS | Transient voltage suppressor | TBD | TBD (2) |
| MOV | Varistor | Littelfuse, Inc. | TMOV20RP300E |
| HV capacitor | High-voltage capacitor | Illinois Capacitor, Inc | 474MKP275KA (3) |

(1) Select the Zener breakdown voltage at the lowest available rating beyond the normal power supply operating range. For example, 1SMB5931B is designed for systems where PA_VS = 15 V, whereas 1SMB5934B is designed for systems where PA_VS = 20 V.
(2) Select the TVS breakdown voltage at or slightly less than (0.5 × PA_VS). For example, SMCJ6.0CA is designed for systems where PA_VS = 15 V, whereas SMCJ8.0CA is designed for systems where PA_VS = 20 V.
(3) A common value for the high-voltage capacitor is 470 nF. Other values may be substituted depending on the application requirements. When making a substitution, the capacitor must be selected from the same family or an equivalent family of capacitors rated to withstand high-voltage surges on the power line for reliability.

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## 9 Power Supply Recommendations

Two power supply pins and two ground pins are available to provide a path for the high currents associated with driving the low impedance of the AC mains. TI recommends connecting the two supply pins together. Placing a 47-μF to 100-μF bypass capacitor in parallel with a 100-nF capacitor as close to the device as possible is also recommended. Take care when routing the high-current ground lines on the PCB to avoid voltage drops in the PCB ground that may vary with changes in load current.

# 10 Layout

## 10.1 Layout Guidelines

### 10.1.1 Thermal Considerations

In a typical power line communications application, the device dissipates 2 W of power when transmitting to the low-impedance AC line. This amount of power dissipation can increase the junction temperature, which can lead to a thermal overload that results in signal transmission interruptions if the PCB thermal design is not implemented properly. Proper management of heat flow from the device and good PCB design and construction are required to ensure proper device temperature, maximize performance, and extend the operating life of the device.

The device is assembled in a 5-mm × 5-mm, QFN-20 package. This QFN package has a large exposed thermal pad on the underside that conducts heat away from the device and to the underlying PCB.

Some heat is conducted from the silicon die surface through the plastic packaging material and is transferred to the ambient environment. However, this route is not the primary thermal path for heat flow because plastic is a relatively poor conductor of heat. Heat flows across the silicon die surface to the bond pads through the wire bonds to the package leads, to the top layer of the PCB. While these paths for heat flow are important, the majority (nearly 80%) of the heat flows downward through the silicon die to the thermally-conductive die-attach epoxy and to the exposed thermal pad on the underside of the package (as shown in Figure 5). Minimizing the thermal resistance of this downward path to the ambient environment maximizes the life and performance of the device.

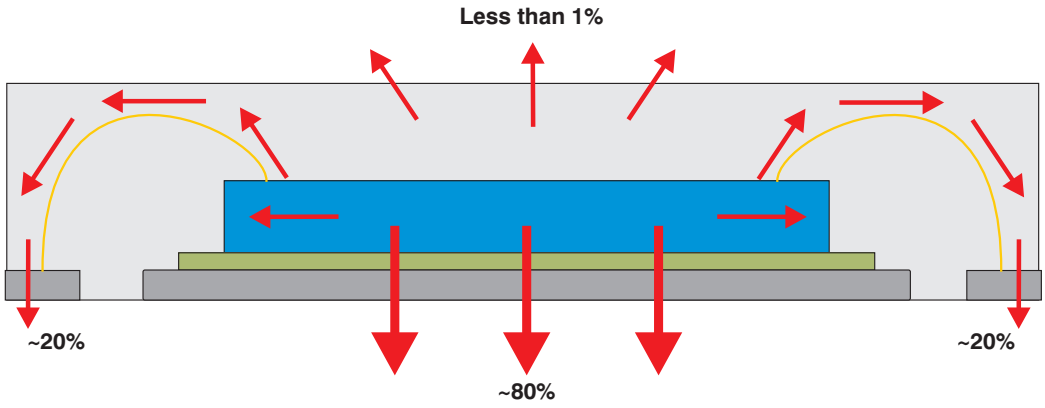


**Figure 5. Heat Flow in the QFN Package**

The exposed thermal pad must be soldered to the PCB thermal pad. The thermal pad on the PCB must be the same size as the exposed thermal pad on the underside of the QFN package. See *QFN/SON PCB Attachment* for recommendations on attaching the thermal pad to the PCB. Figure 6 shows the direction of heat spreading to the PCB from the device.

## Layout Guidelines (continued)

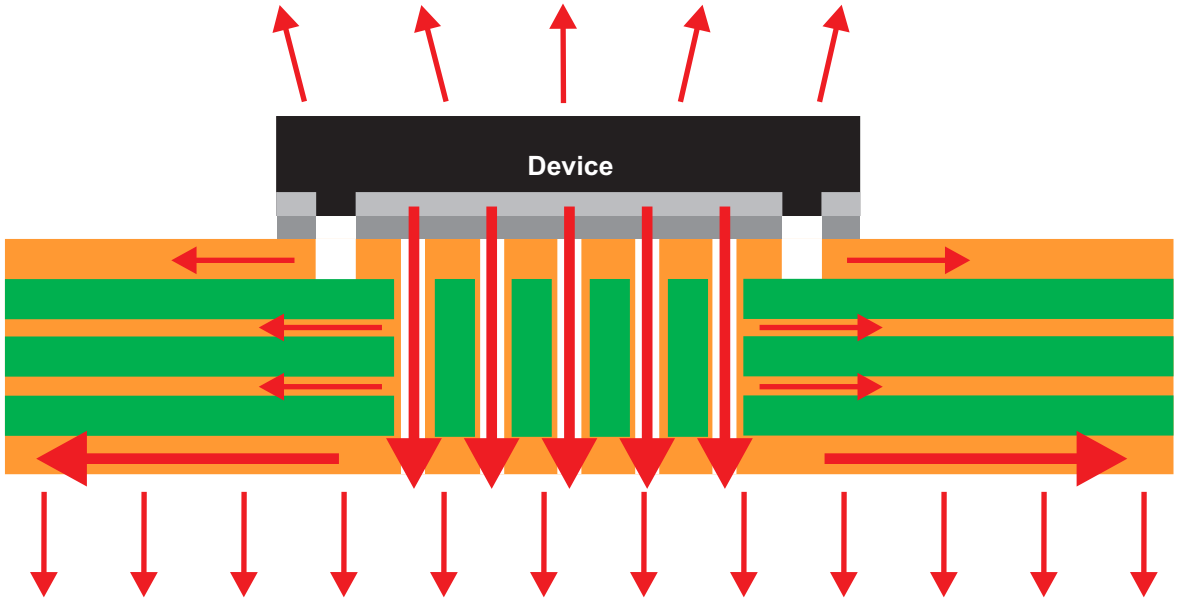


**Figure 6. Heat Spreading to PCB**

The heat spreading to the PCB is maximized if the thermal path is uninterrupted. Best results are achieved if the heat-spreading surfaces are filled with copper to the greatest extent possible, which maximizes the percentage of area covered on each layer. As an example, a thermally robust, multilayer PCB design consists of four layers with copper (Cu) coverage of 60% in the top layer, 85% and 90% in the inner layers (respectively), and 95% on the bottom layer.

Increasing the number of layers in the PCB, using thicker copper, and increasing the PCB area are all factors that improve the spread of heat. Figure 7 through Figure 9 show thermal resistance performance as a function of each of these factors.

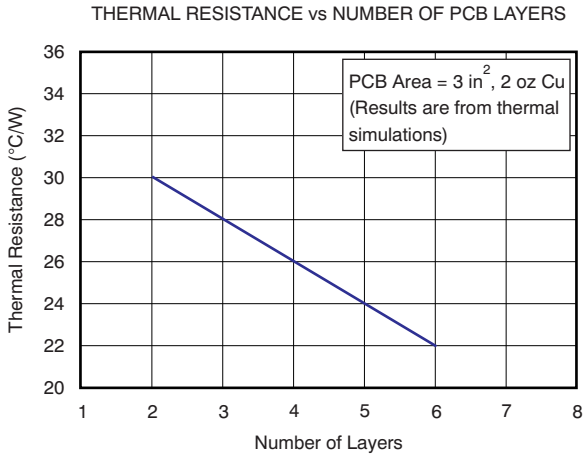


**Figure 7. Thermal Resistance as a Function of the Number of Layers in the PCB**

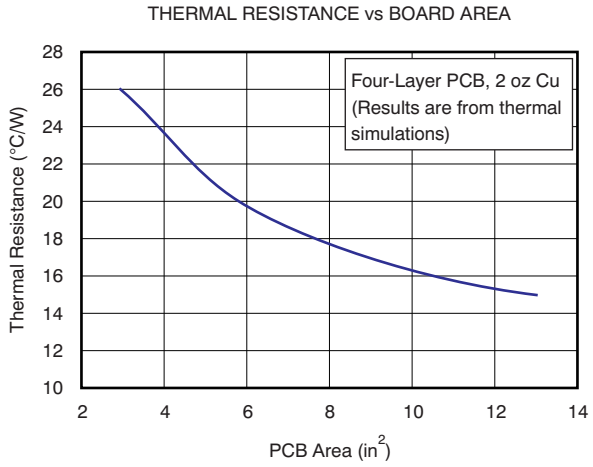


**Figure 8. Thermal Resistance as a Function of PCB Area**

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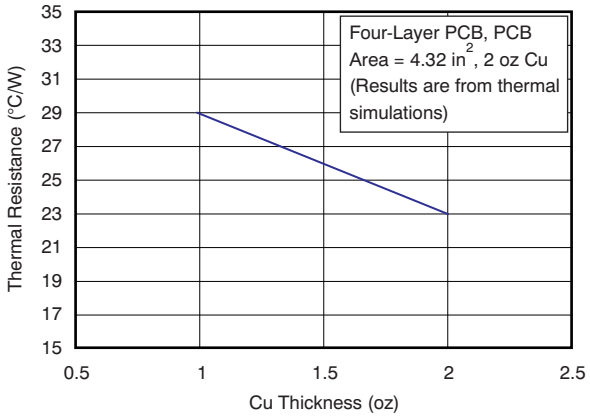


**Figure 9. Thermal Resistance as a Function of Copper Thickness**

For additional information on thermal PCB design using exposed thermal pad packages, see *PowerPAD™ Thermally-Enhanced Package* (available for download at www.ti.com).

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## 10.2 Layout Example

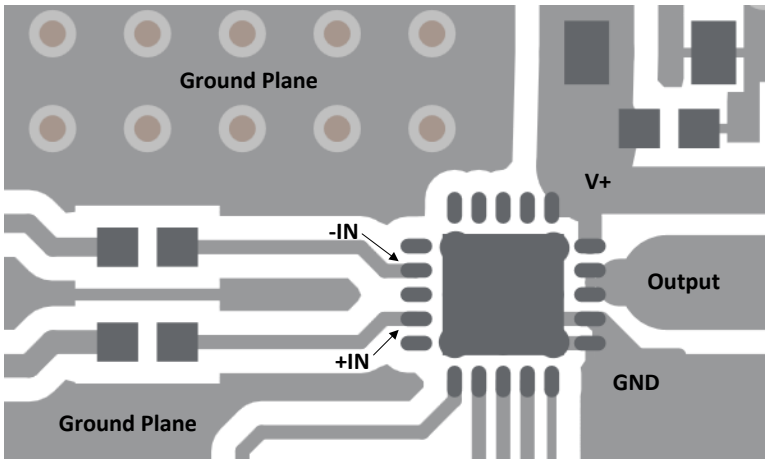


**Figure 10. Recommended Layout for Typical Transformer Coupling Application**

# 11 Device and Documentation Support

## 11.1 Documentation Support

### 11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *PowerPAD™ Thermally Enhanced Package*
- Texas Instruments, *QFN/SON PCB Attachment*

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA521IRGWR | PREVIEW | VQFN | RGW | 20 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | |
| OPA521IRGWT | PREVIEW | VQFN | RGW | 20 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |
| POPA521IRGWT | ACTIVE | VQFN | RGW | 20 | 250 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

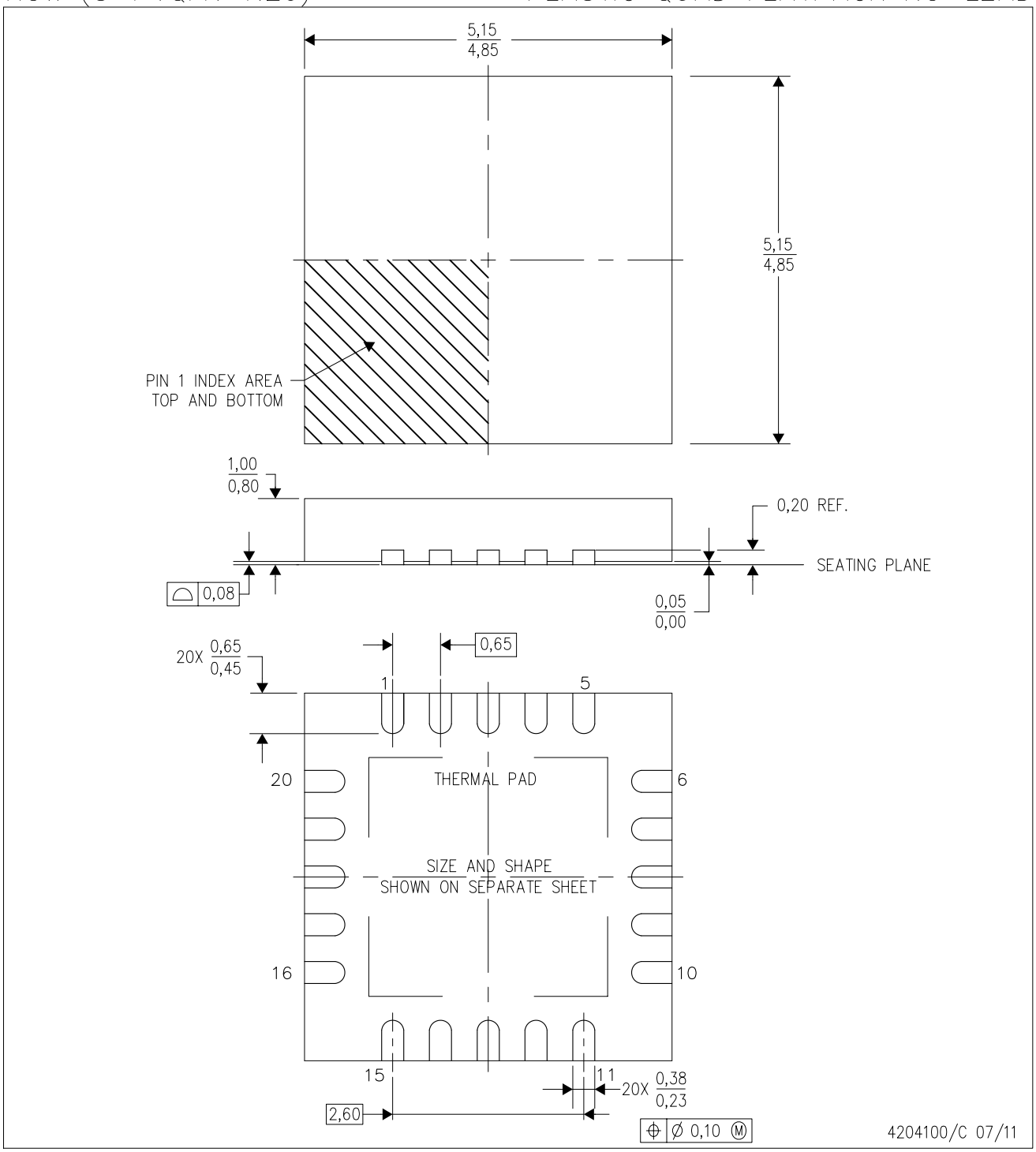
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RGW (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flat pack, No–leads (QFN) package configuration
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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