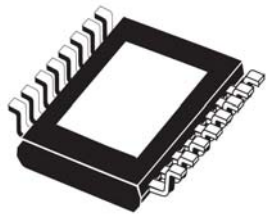
L99MC6GJ

Automotive configurable 6-channel device

Datasheet - production data



PowerSSO-16

Features

- AEC-Q100 qualified
- 3 independently self configuring high-/low-side channels
- 3 low-side channels
- R_{ON} = 0.7 Ω (typ) at T_j = 25 °C
- Current limit of each output at min. 0.6 A
- PWM direct mode
- Bulb mode with recovery mode
- LED mode with slew rate control
- Bridge mode with crosscurrent protection
- SPI interface for data communication
- Temperature warning
- All outputs overtemperature protected
- All outputs short-circuit protected
- Configurable open-load detection in off mode
- V_{CC} supply voltage 3.0 V to 5.25 V
- Very low current consumption in standby mode 5 µA (typ)
- Internal clamp diodes
- HS switches operate down to 3 V crank voltage

Applications

- Relay driver
- LED driver
- Motor driver
- Mirror adjustment

Description

The L99MC6GJ IC is a highly flexible monolithic medium current output driver that incorporates 3 dedicated low-side outputs (channels 4 to 6) and 3 independently self configuring outputs (channels 1 to 3) that can be used as either low-side or high-side drivers in any combination. The L99MC6GJ can control inductive loads, incandescent bulbs or LEDs.

The L99MC6GJ can be used in a half bridge configuration with crosscurrent protection.

The channel 2 can be controlled directly via the IN/PWM pin for PWM applications. The IN/PWM signal can be applied to any other output.

The integrated 16-bit standard serial peripheral interface (SPI) controls all outputs and provides diagnostic information: normal operation, open-load in off-state, overcurrent, temperature warning, overtemperature.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-16	L99MC6GJ	L99MC6GJTR

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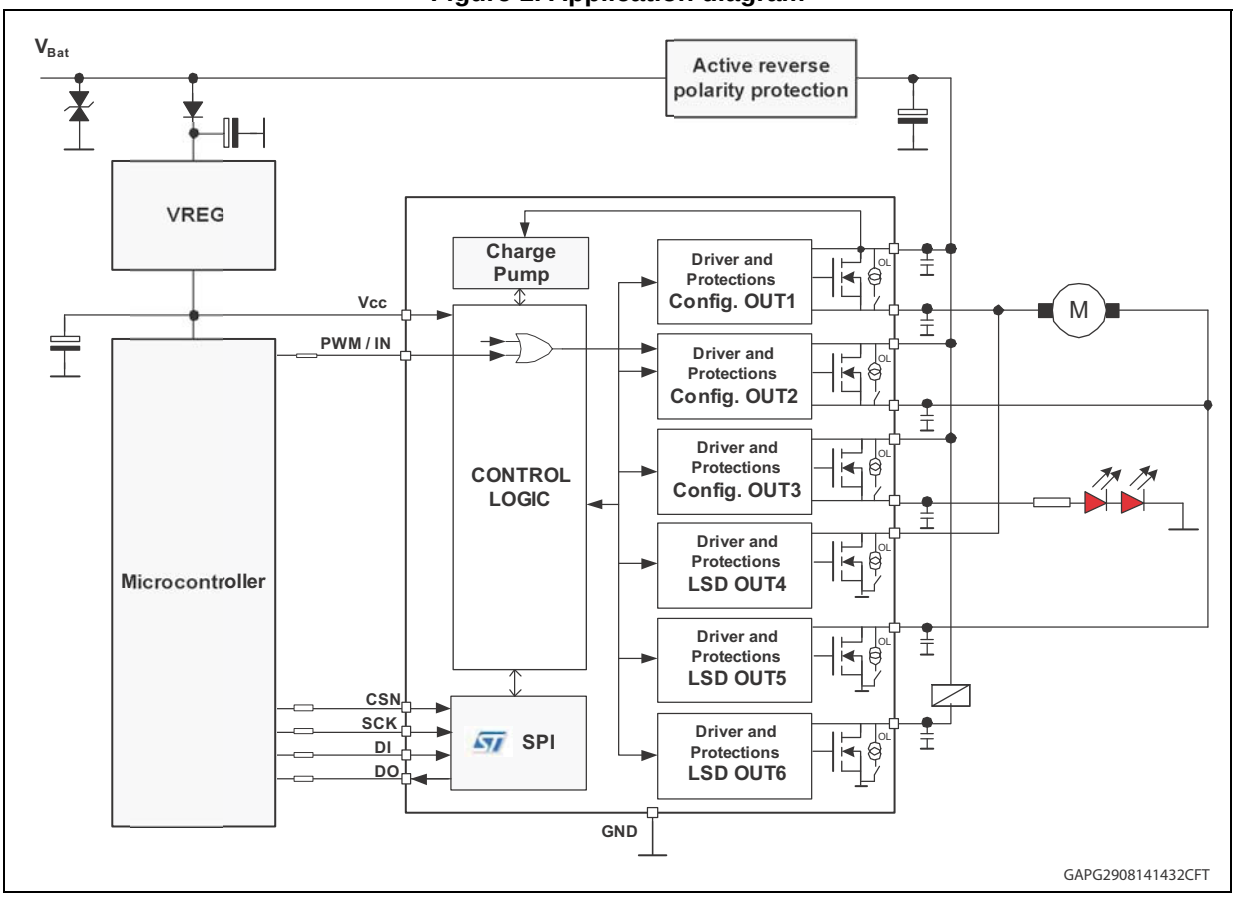
1 Introduction

1.1 Application diagram

Figure 1. Application diagram



1.2 Block diagram and pin description

Figure 2. Block diagram

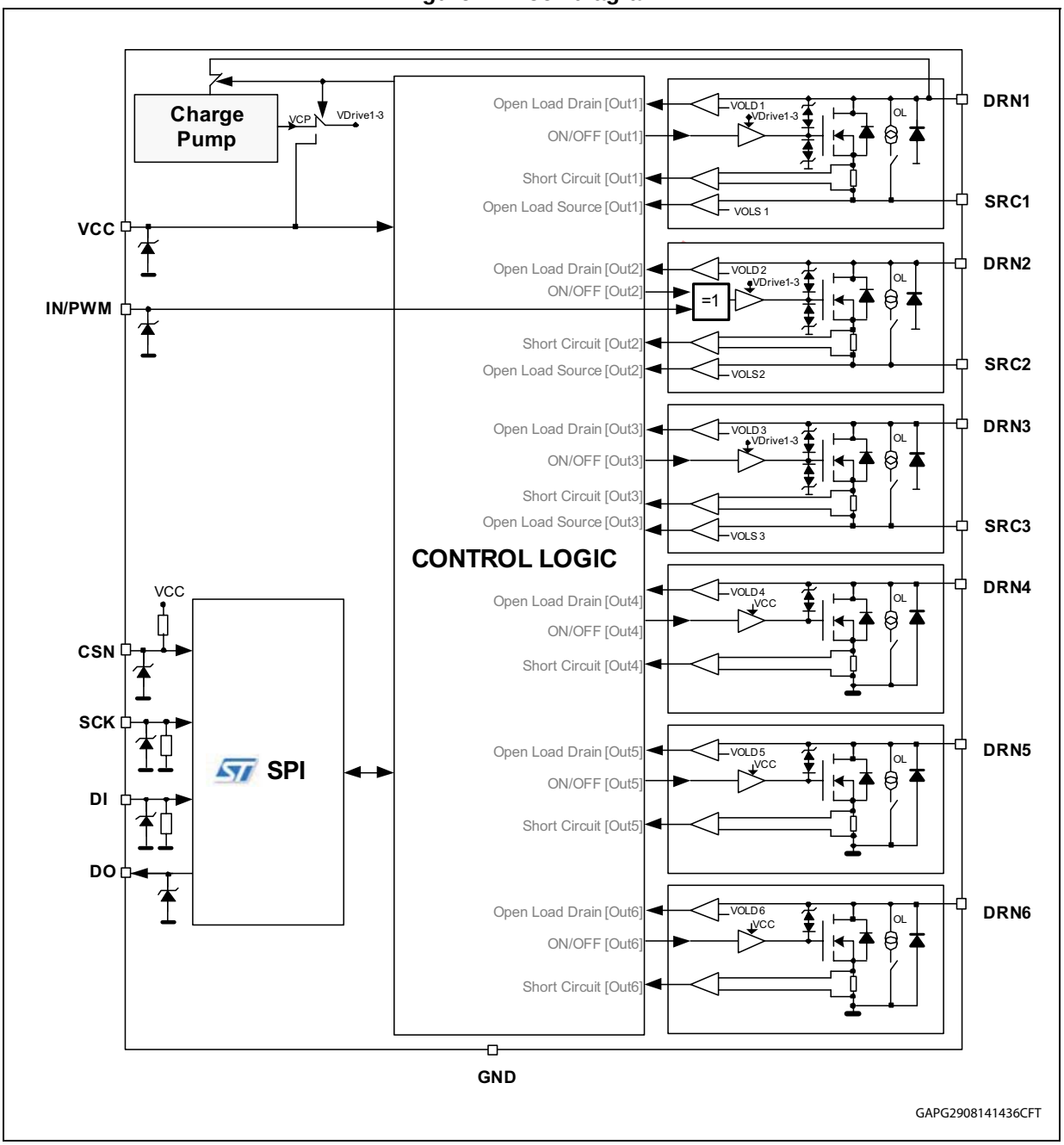
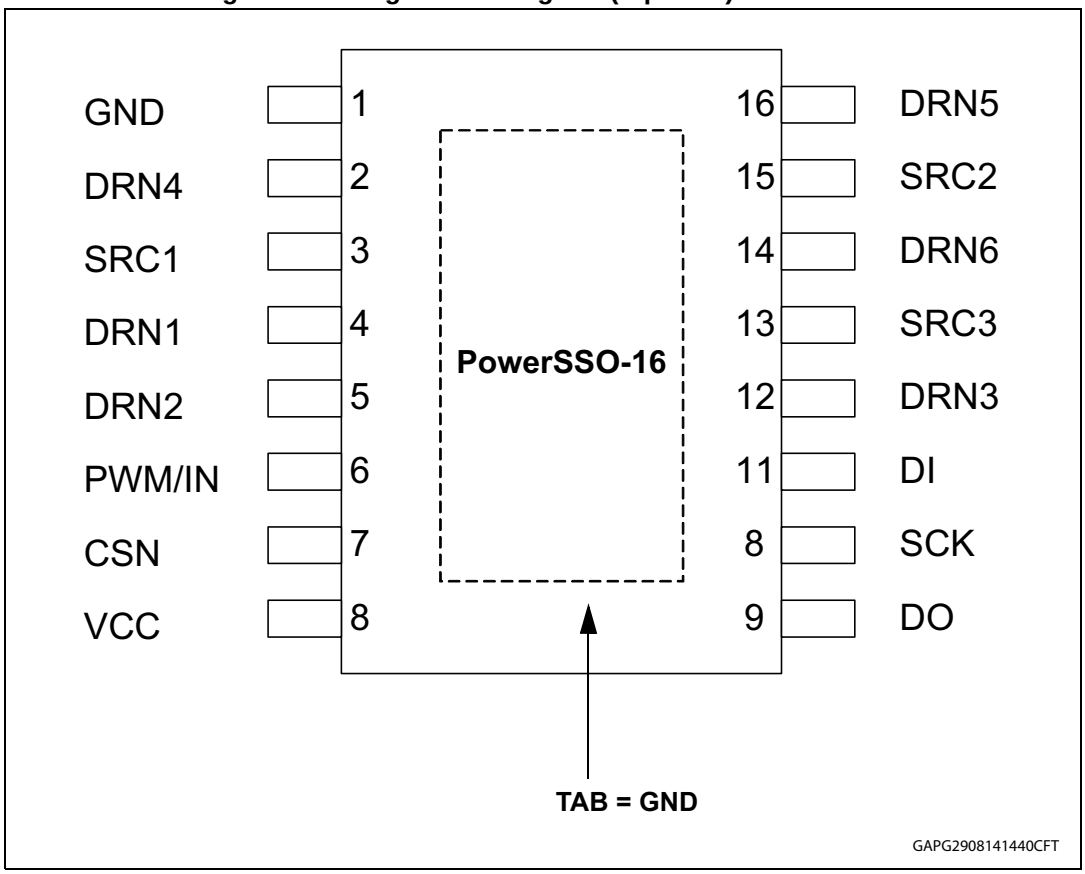


Table 2. Pin functions

Pin	Symbol	Function
1 / TAB	GND	**Ground**: Reference potential
6	IN/PWM	**IN/PWM direct mode:** Direct input for channel 2. Other channels can be driven in PWM mode via SPI.
8	VCC	**Logic voltage supply 3.3 V/5 V:** For this input a ceramic capacitor as close as possible to GND is recommended
3	SRC1	Source of configurable channel 1
4	DRN1	Drain of self configurable channel 1, in HS mode also V_S supply
5	DRN2	Drain of self configurable channel 2
15	SRC2	Source of self configurable channel 2
12	DRN3	Drain of self configurable channel 3
13	SRC3	Source of self configurable channel 3
2	DRN4	Drain of channel 4
16	DRN5	Drain of channel 5
14	DRN6	Drain of channel 6
11	DI	**SPI data in:** The input requires CMOS logic levels and receives serial data from the microcontroller. The data is a 16-bit control word and the most significant bit (MSB, bit 7) is transferred first.
9	DO	**SPI data out:** The diagnosis data is available via the SPI and this tristate-output. The output remains in tristate, if the chip is not selected by the input CSN (CSN = high).
7	CSN	**SPI chip select not (active low):** This input is low active and requires CMOS logic levels. The serial data transfer between the L99MC6GJ and microcontroller is enabled by pulling the input CSN to low-level.
10	SCK	**SPI serial clock input:** This input controls the internal shift register of the SPI and requires CMOS logic levels.

Figure 3. Configuration diagram (top view) not in scale

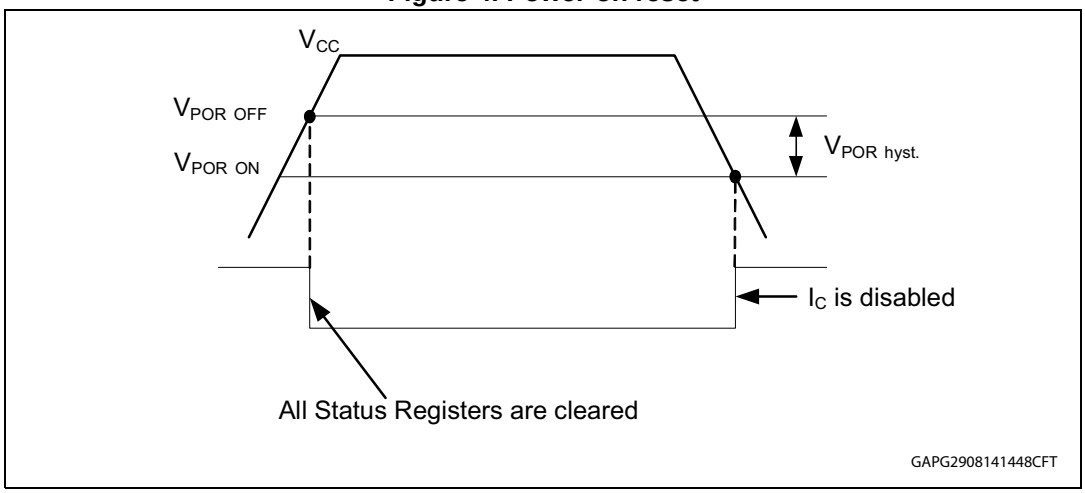


2 Description

2.1 Dual power supply: V_S and V_{CC}

The supply voltage V_{CC} (3.3 V/5 V) supplies the whole device. In case of power-on (V_{CC} increases from undervoltage to $V_{POR\ OFF}$ = 2.7 V, typical) the circuit is initialized by an internally generated power-on reset (POR). If the voltage V_{CC} decreases under the minimum threshold ($V_{POR\ ON}$ = 2.4 V, typical), the outputs are switched-off (high-impedance) and the status registers are cleared (see *Figure 4*).

Figure 4. Power-on reset



2.1.1 Channels

The channels 1 to 3 are self configuring high-side or low-side n-channel mosfets. This flexibility allows the user to connect loads in high-side or low-side configuration in any combination.

In order to provide low R_{dson} values for high-side configured switches (channels 1 to 3), a charge pump (CP) to drive the internal gate voltage(s) is implemented. If the charge pump is activated (ENCP1 = 1, DISCP2 = 0, see *Section 9.3: Control and status registers*), the internal charge-pump uses V_S from the drain of channel 1, as its power source. Otherwise V_{CC} is used to drive all channels.

The channels 4 to 6 are n-channel low-side drivers. The source of the respective mosfet are internally connected to the device GND.

Caution: For any high-side configuration, channel 1 must be used as a high-side switch. If channel 1 is configured as low-side, the charge pump has to be deactivated to avoid charge pump current from the drain.

Caution: The charge pump may not be deactivated (see *Section 9.3: Control and status registers*) if one of the channels is in high-side configuration, while a short-circuit from the source to the battery is present. If these conditions occur, the voltage of the shorted source is applied to the VCC pin.

2.2 Standby mode

The standby mode of the L99MC6GJ is activated by SPI command (EN bit of CTRL 0 reset to 0, see *Section 9.3.2: Register description*). The inputs and outputs are switched-off. The status registers are cleared and the control registers are reset to their default values.

In the standby mode the current consumption is 5 µA (typical value). A SPI command is needed to switch the L99MC6GJ in normal mode.

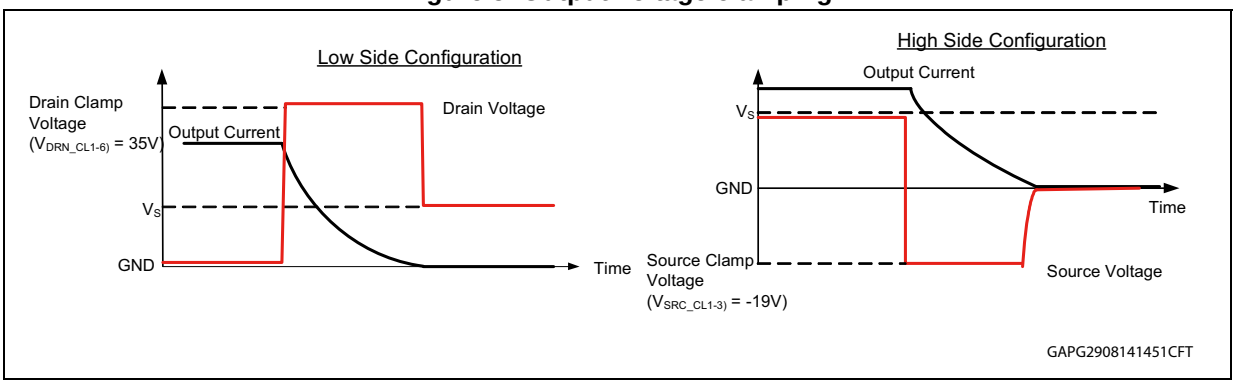
2.3 Inductive loads

Each switch is built by a power DMOS transistor. For low-side configured outputs an internal zener clamp from the drain to gate with a breakdown of 31 V minimum provides for fast turn-off of inductive loads.

For high-side configured outputs, an internal zener clamp with a breakdown of -15 V maximum provides for fast turn-off of inductive loads (*Figure 5*).

The maximum clamping energy is specified in *Chapter 10*.

Figure 5. Output voltage clamping



2.4 Diagnostic functions

All diagnostic functions (overload, open-load, temperature warning and thermal shutdown) are internally filtered and the condition has to be valid for at least 32 µs (open-load: typ. 400 µs, respectively) before the corresponding status bit in the status registers are set. The filters are used to improve the noise immunity of the device. Open-load and temperature warning function are intended for information purpose and do not change the state of the output drivers. On contrary, the overload and thermal shutdown condition disable the corresponding driver (overload) or all drivers (thermal shutdown), respectively. Without setting the overcurrent recovery bit in the input data register to logic high, the microcontroller has to clear the overcurrent status bit to reactivate the corresponding driver. (All switches have a corresponding overcurrent recovery bit) If this bit is set, the device automatically switches-on the outputs again after a short recovery time. With this feature the device can drive loads with start-up currents higher than the overcurrent limits (that is inrush current of incandescent lamps, cold resistance of motors and heaters, *Figure 7*).

2.4.1 Direct input IN/PWM

The IN/PWM input allows channel 2 to be enabled without the use of SPI. The IN/PWM pin is OR-ed with the SPI command bit. This pin can be left open if the channel 2 is controlled only via the SPI. This input has an internal pull-down.

The IN/PWM signal can also be applied to any other switches by the activation of the PWM mode.

This input is suited for non-inductive loads that are pulse width modulated. This allows PWM control without further use of the SPI.

2.4.2 Temperature warning and thermal shutdown

If the junction temperature rises above $T_{j\ TW}$ a temperature warning flag is set and is detectable via the SPI. If the junction temperature increases above the second threshold $T_{j\ SD}$, the thermal shutdown bit is set and power DMOS transistors of all output stages are switched-off to protect the device. Temperature warning flag and thermal shutdown bits are latched. In order to reactivate the output stages, the junction temperature must decrease below $T_{j\ SD}$ - $T_{j\ SD\ HYS}$ and the thermal shutdown bit has to be cleared by the microcontroller.

2.4.3 Open-load detection in off-state

The open-load detection monitors the load at each output stage in off mode. A current source of 150 µA (I_{OLD1-6}, $I_{OLS\ 1-3}$) is connected between drain and source or GND. An open-load failure is detected if the drain or source voltage reaches an internal $V_{OLD/S}$ (2.0 V) for at least 3 ms ($t_{dOL\ typ.}$). The corresponding open-load bit is set in the status register. In LED mode the open-load detection is disabled and the current source is switched-off, which avoids a turn-on of the LEDs in off-state.

2.4.4 Overload detection

In case of an overcurrent condition, a flag is set in the corresponding status register. If the overcurrent signal is valid for at least t_{ISC} = 32 µs, the overcurrent flag is set and the corresponding driver is switched-off to reduce the power dissipation and to protect the integrated circuit. If the overcurrent recovery bit of the output is zero the microcontroller has to clear the status bit to reactivate the corresponding driver.

2.5 Bridge mode

The L99MC6GJ can be configured as bridge driver. Up to three half bridges can be used. In Bridge mode the device is crosscurrent protected by an internal delay time. If one driver (LS or HS) is turned-off the activation of the other driver of the same half bridge is automatically delayed by the crosscurrent protection time. After the crosscurrent protection time is expired the slew rate limited switch-off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned-on with slew-rate limitation. Due to this behavior it is always guaranteed that the previously activated driver is totally turned-off before the opposite driver starts to conduct.

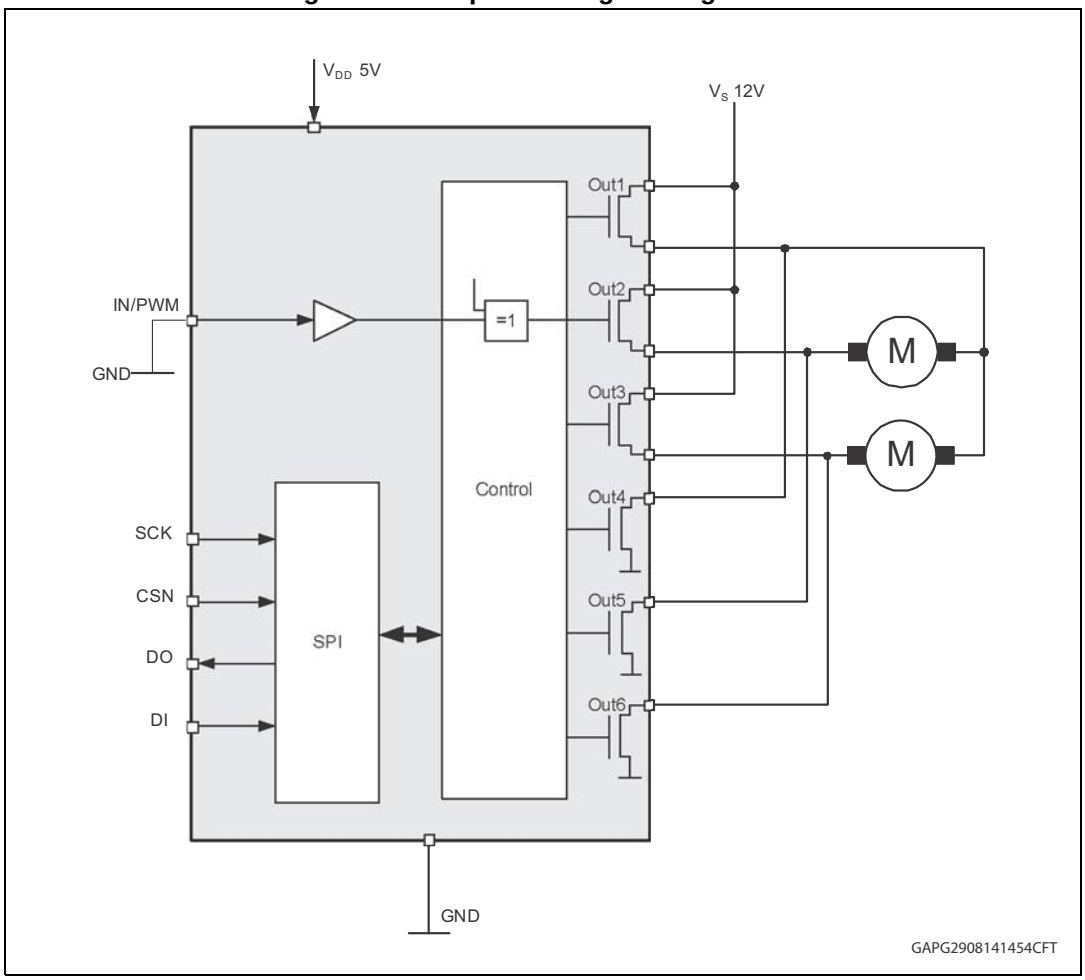
Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs without external free-wheeling diodes.

The following combination must be used: channel 1 + 4, channel 2 + 5, channel 3 + 6 (*Figure 6*).

A V_S voltage exceeding the low-side clamping voltage (V_{DRN_CL1-6}) , while the high one of the high-side drivers is turned on, may cause a destruction of the device.

Caution: In bridge mode using channels 2 and 5, the IN/PWM pin has to be grounded. Therefore PWM mode on other channels is not possible.

Figure 6. Example of bridge configuration



2.6 LED mode

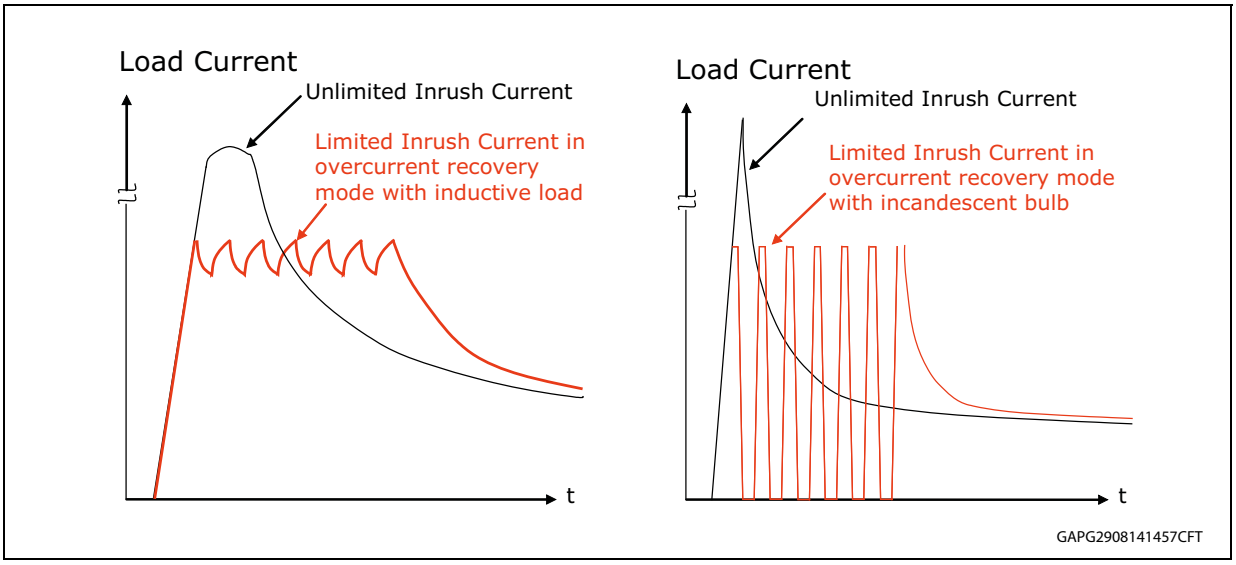
Open-load detection in off-state can be deactivated to avoid the turn on of the LEDs by the current source (150 µA typ.) when the channel is switched-off.
Moreover, it is possible to select a high slew rate to support PWM operations with small duty cycle (see *Section 9.3.1: Channel configuration decoding*).

2.7 Bulb mode (programmable soft start function to drive loads with higher inrush current)

Loads with start-up currents higher than the overcurrent limits (for example inrush current of lamps, start current of motors and cold resistance of heaters) can be driven by using the programmable soft start function (that is overcurrent recovery mode). Each driver has a corresponding overcurrent recovery bit. If this bit is set, the device automatically switches-on the outputs again after a fixed recovery time. The PWM modulated current provides sufficient average current to power up the load (for example heat up the bulb) until the load reaches operating condition (*Figure 6*).

The device itself cannot distinguish between a real overload and a non linear load like a light bulb. A real overload condition can only be qualified by time. As an example the microcontroller can switch-on light bulbs by setting the overcurrent recovery bit for the first 50 ms. After clearing the recovery bit, the output is automatically disabled if the overload condition still exits.

Figure 7. Example of programmable soft start function for inductive loads and incandescent bulbs



3 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S (DRN1 HS config)	DC supply voltage	-0.3 to 28	V
	Single pulse t_{max} < 400 ms in HS or LS configuration with $R_{load\ min}$ = 40 Ω(1)	40	V
	Single pulse t_{max} < 400 ms in bridge mode	V_{DRN_CL1-6}	V
V_{CC}	Stabilized supply voltage, logic supply	-0.3 to 5.5	V
DI, DO, SCK, CSN, IN	Digital input/output voltage	-0.3 to V_{CC} + 0.3	V
DRN 1-6	Output current capability	±1,65	A
SRC 1-3	Output current capability	±1,65	A
GND	Current capability	3,30	A
T_j	Operating junction temperature	-40 to 150	°C

1. The device requires a minimum load impedance of 40 Ω to sustain a load dump pulse of 40 V according to the ISO 7637 pulse 5b.

All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit.

4 ESD protection

Table 4. ESD protection

Parameter	Value	Unit
All pins	±2(1)	kV
Output pins: DRN1 – DRN6; SRC1, SRC3, SRC5	±4(2)	kV
Machine model (CDF-AEC-Q100-03 rev. F)	±200	V
Charged device model (CDF-AEC-Q100-011 Rev. F)	±1000	V

1. HBM according to MIL 883C, Method 3015.7 or EIA/JESD22-A114-A
2. HBM with all unzapped pins grounded

5 Thermal data

5.1 Temperature warning and thermal shutdown

Table 5. Temperature warning and thermal shutdown

Item	Symbol	Parameter		Min.	Typ.	Max.	Unit
5.2.1	$T_{jTW\ ON}$	Temperature warning threshold junction temperature	T_j increasing			150	°C
5.2.2	$T_{jTW\ OFF}$	Temperature warning threshold junction temperature	T_j decreasing	130			°C
5.2.3	$T_{jTW\ HYS}$	Temperature warning hysteresis	-		5		K
5.2.4	$T_{jSD\ ON}$	Thermal shutdown threshold junction temperature	T_j increasing			170	°C
5.2.5	$T_{jSD\ OFF}$	Thermal shutdown threshold junction temperature	T_j decreasing	150			°C
5.2.6	$T_{jSD\ HYS}$	Thermal shutdown hysteresis	-		5		K

For additional information, please refer to *Chapter 12: Package and PCB thermal data*.

6 Electrical characteristics

V_S = 6 V to 16 V, V_{CC} = 3.0 V to 5.3 V, T_j = -40 °C to 150 °C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6.1 Supply

Table 6. Supply

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
6.1.1	V_S	Operating supply voltage range		6		28	V
6.1.2	I_S	V_S DC supply current	V_S = 13 V, V_{CC} = 5.0 V active mode DRN1 = V_S Outputs floating		1.5	2.0	mA
6.1.3	I_{VS}	V_S quiescent supply current	V_S = 13 V, V_{CC} = 5 V standby mode DRN1 = V_S T_{Test} = -40 °C, 25 °C; Outputs floating		3	10	µA
			T_{Test} = 130 °C		6	20	µA
6.1.4	V_{CC}	Operating supply voltage range		3.0		5.3	V
6.1.5	I_{CC}	V_{CC} DC supply current	V_S = 13 V, V_{CC} = 5.0 V active mode		1.3	2	mA
6.1.6		V_{CC} quiescent supply current	V_S = 13 V, V_{CC} = 5.0 V; CSN = V_{CC}; standby mode Outputs floating		5	20	µA

6.2 Undervoltage detection

Table 7. Undervoltage detection

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
6.2.1	$V_{POR\ OFF}$	Power-on reset threshold	V_{CC} increasing			3.0	V
6.2.2	$V_{POR\ ON}$	Power-on reset threshold	V_{CC} decreasing	2.2			V
6.2.3	$V_{POR\ hyst}$	Power-on reset hysteresis	$V_{POR\ OFF}$ - $V_{POR\ ON}$		0.3		V

6.3 Channels

Table 8. Channels

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
6.3.1	$r_{ON\ SWI1-3}$	On resistance drain to source in HS configuration	V_S=13.5 V, T_j = 25 °C, CP on, I_{load} = 250 mA	—	700	900	mΩ
			V_S=13.5 V, T_j = 125 °C, CP on, I_{load} = 250 mA	—	1100	1500	mΩ
			V_S = 6.0 V T_j = 25 °C, CP on, I_{load} = 125 mA	—	700	900	mΩ
			V_S = 6.0 V, T_j = 125 °C, CP on, I_{load} = 125 mA	—	1100	1500	mΩ
			V_S = 4.5 V T_j = 25 °C, CP on, I_{load} = 125 mA	—	800	1500	mΩ
			V_S = 4.5 V, T_j = 125 °C, CP on, Load = 125 mA	—	1300	2000	mΩ
			V_S = 3 V, T_j = 25 °C, CP on, I_{load} = 125 mA	—	1600	2600	mΩ
6.3.2	$r_{ON\ SWI1-6}$	On resistance drain to source or GND, in LS configuration	V_{CC}=5.0 V, T_j = 25 °C, Load = 250 mA	—	750	1000	mΩ
			V_{CC} = 5.0 V, T_j = 125 °C, I_{load} = 250 mA	—	1100	1500	mΩ
			V_{CC} = 3.3 V, T_j = 25 °C, I_{load} = 250 mA	—	900	1250	mΩ
			V_{CC} = 3.3 V, T_j = 125 °C, I_{load} = 250 mA	—	1400	1800	mΩ
6.3.3	I_{SC1-6}	Overcurrent protection	Channels 1 to 3	0.7	1.0	1.4	A
			Channels 4 to 6	0.6	0.8	1.0	A
6.3.4	$t_{d\ ON1-6}$	Output delay time, switch-on	V_S = 13.5 V, V_{CC} = 5.0 V	—	50	100	µs
6.3.5	$t_{d\ OFF1-6}$	Output delay time, switch-off	V_S = 13.5 V, V_{CC} = 5.0 V	—	50	100	µs
6.3.6	$t_{d\ ONLED1-6}$	Output delay time, switch-on LED	V_S = 13.5 V, V_{CC} = 5.0 V	—	15	40	µs
6.3.7	$t_{dOFFLED1-6}$	Output delay time, switch-off LED	V_S = 13.5 V, V_{CC} = 5.0 V	—	15	40	µs
6.3.8	t_{DHL}	Crosscurrent protection time	Only in Bridge mode	—	200	500	µs
6.3.9	I_{QLD}	Switched-off output current DRN 1-6	V_{DRN2-6} = V_S, LED mode, CP off	0	—	5	µA
			V_{DRN1}	—	20		µA
6.3.10	I_{QLS}	Switched-off output current SRC 1-3	V_{SRC1-3} = GND, LED mode	—	-15	-25	µA

Table 8. Channels (continued)

Item	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
6.3.11	V_{OLD1-6}	Drain open-load detection voltage on drain		1,1	2,0	2,5	V
6.3.12	I_{OLD1-6}	Open-load detection current on drain	@ V_{OLD}	80	190	280	µA
6.3.13	V_{OLS1-3}	Source open-load detection voltage on source		1,1	2,0	2,5	V
6.3.14	I_{OLS1-3}	Open-load detection current on source	@ V_{OLS}	-80	-190	-280	µA
6.3.15	t_{dOL}	Minimum duration of open-load condition to set the status bit	Guaranteed by design	2	3	4	ms
6.3.16	t_{ISC}	Minimum duration of overcurrent condition to switch-off the driver	Guaranteed by design	10	—	100	µs
6.3.17	dV_{OUT1}/dt	Slew rate of channel 1 to 6	V_S = 13.5 V, V_{CC} = 5.0 V; I_{load} = 54 Ω	0.1	0.25	0.4	V/µs
6.3.18	$dV_{OUT1LED}/dt$	Slew rate of channel 1 to 6 in LED mode	V_S = 13.5 V, V_{CC} = 5.0 V I_{load} = 54 Ω	0.5	1.25	2.0	V/µs
6.3.19	V_{DRN_CL1-6}	Drain clamp voltage (low-side)	Source = GND I_{load} = 0.25 A	31	35	39	V
6.3.20	V_{SRC_CL1-3}	Source clamp voltage (high-side)	Drain = V_S, I_{load} = 0.25 A	-22	-19	-15	V
			Standby	-22	10	-1,5	V

7 SPI electrical characteristics

V_S = 6 V to 16 V, V_{CC} = 3.0 V to 5.3 V, T_j = -40 °C to 150 °C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin

7.1 DC characteristics

Table 9. DC characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
DI, SCK, CSN, PWM						
V_{IL}	Low-level input voltage	—			$0.3V_{DD}$	V
V_{IH}	High-level input voltage	—	$0.7V_{DD}$			V
$R_{CSN\ in}$	Pull-up resistor at input CSN	—	20	50	80	kΩ
$R_{CLK\ in}$	Pull-down resistor at input CLK	—	20	50	80	kΩ
$R_{DI\ in}$	Pull-down resistor at input DI	—	20	50	80	kΩ
DO						
V_{OL}	Low-level output voltage	I_{OUT} = 5 mA			$0.3V_{DD}$	V
V_{OH}	High-level output voltage	I_{OUT} = 5 mA	$0.7V_{DD}$			V

7.2 AC characteristics

Table 10. AC characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
DI, DO, SCK, CSN						
C_{OUT}	Output capacitance (DO)	V_{OUT} = 0 to 5 V	—	—	10	pF
C_{IN}	Input capacitance (DI)	V_{IN} = 0 to 5 V	—	—	10	pF
	Input capacitance (other pins)	V_{IN} = 0 to 5 V	—	—	10	pF

7.3 Dynamic characteristics

Table 11. Dynamic characteristic

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
f_C	Clock frequency	—	—	—	1	MHz
t_{SCSN}	CSN low setup time	See *Figure 8*	120	—	—	ns
t_{HCSN}	CSN high setup time	See *Figure 8*	1	—	—	µs
t_{CSNQV}	CSN falling until DO valid	—	5	130	250	ns
t_{CSNQT}	CSN rising until DO tristate	—	150	650	1000	ns
t_{SSCK}	SCK setup time before CSN rising	—	200	—	—	ns
t_{SSDI}	Data in setup time	See *Figure 8*	20	—	—	ns
t_{CHDX}	Data hold setup time	See *Figure 8*	30	—	—	ns
t_{HSCK}	SCK high time	See *Figure 8*	115	—	—	ns
t_{LSCK}	SCK low time	See *Figure 8*	115	—	—	ns
t_{SCKQV}	Clock high to output valid	C_{OUT} = 100 pF	—	150	—	ns
t_{QLQH}	Output rise time	C_{OUT} = 100 pF	—	110	—	ns
t_{QHQL}	Output fall time	C_{OUT} = 100 pF	—	110	—	ns
$t_{enDOtriH}$	DO enable time from tristate to high-level	C_{OUT} = 100 pF, I_{OUT} = -1 mA, pull-down load to GND	—	100	250	ns
$t_{enDOtriL}$	DO enable time from tristate to low-level	C_{OUT} = 100 pF, I_{OUT}=1 mA, pull-up load to V_{CC}	—	100	250	ns
$t_{disDOHtri}$	DO disable time from high-level to tristate	C_{OUT} = 100 pF, I_{OUT} = -4 mA, pull-down load to GND	—	625	720	ns
$t_{disDOLtri}$	DO disable time from low-level to tristate	C_{OUT} = 100 pF, I_{OUT} = 4 mA, pull-up load to V_{CC}	—	540	620	ns

7.4 SPI timing parameter definition

Figure 8. Serial input timing

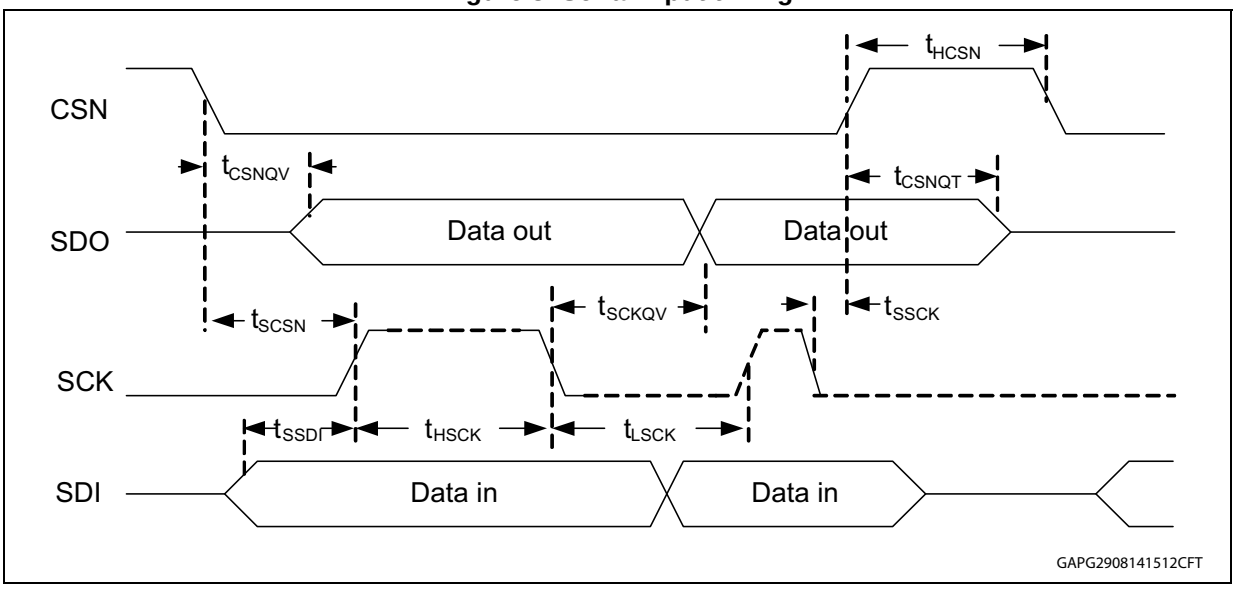


Figure 9. Serial input timing

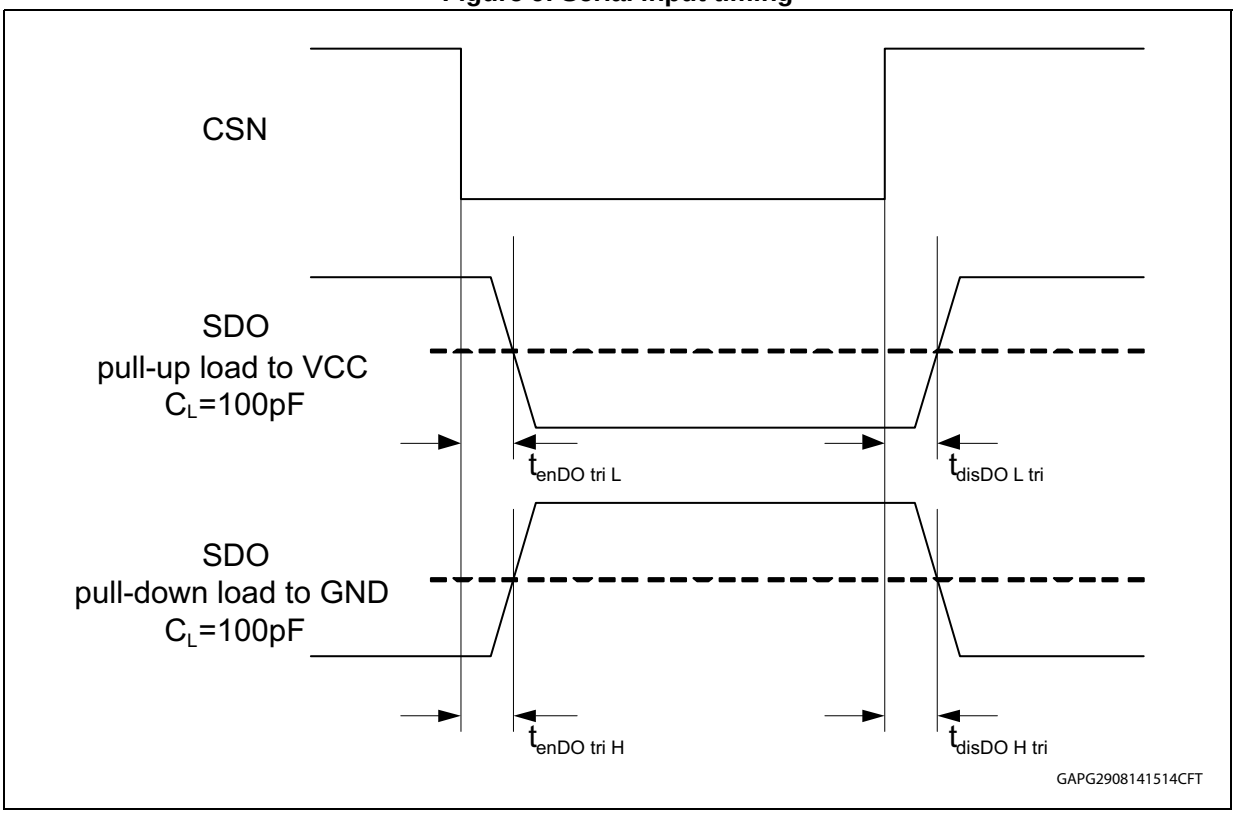
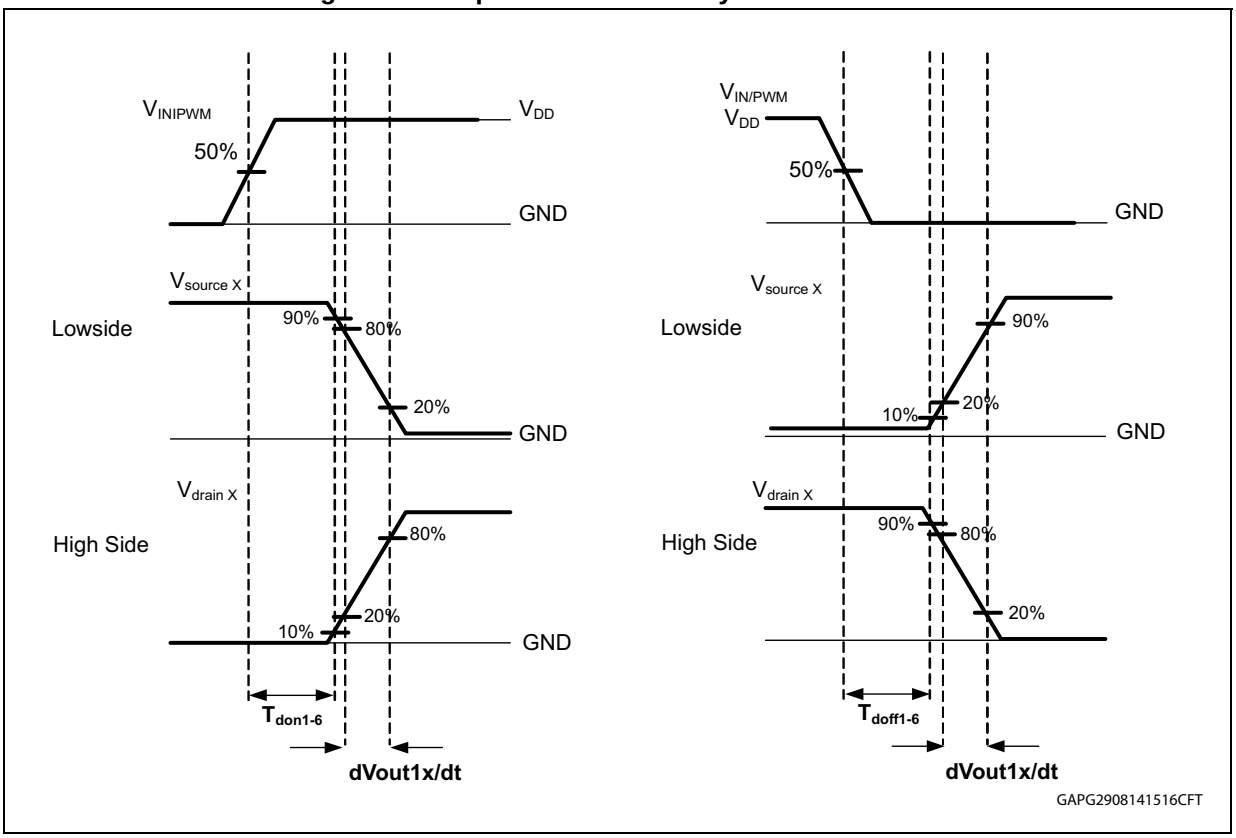


Figure 10. Output turn on/off delays and slew rates



8 Functional description of the SPI

8.1 Signal description

8.1.1 Serial clock (SCK)

This input signal provides the timing of the serial interface. Data present at serial data input (SDI) is latched on the rising edge of serial clock (SCK). Data on serial data output (SDO) is shifted out at the falling edge of serial clock (see *Figure 11*).

The SPI can be driven by a microcontroller with its SPI peripherals running in following mode: CPOL = 0 and CPHA = 0 (see *Figure 11*).

8.1.2 Serial data input (SDI)

This input is used to transfer data serially into the device. It receives the data to be written. Values are latched on the rising edge of serial clock (SCK).

8.1.3 Serial data output (SDO)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of serial clock (SCK).

DO also reflects the status of the <Global Error Flag> (<Global Status Register>, bit 7) while CSN is low and no clock signal is present

8.1.4 Chip select not (CSN)

When this input signal is high, the device is deselected and serial data output (SDO) is high-impedance. Driving this input low enables the communication. The communication must start and stop on a low-level of serial clock (SCK).

Figure 11. Clock polarity and clock phase

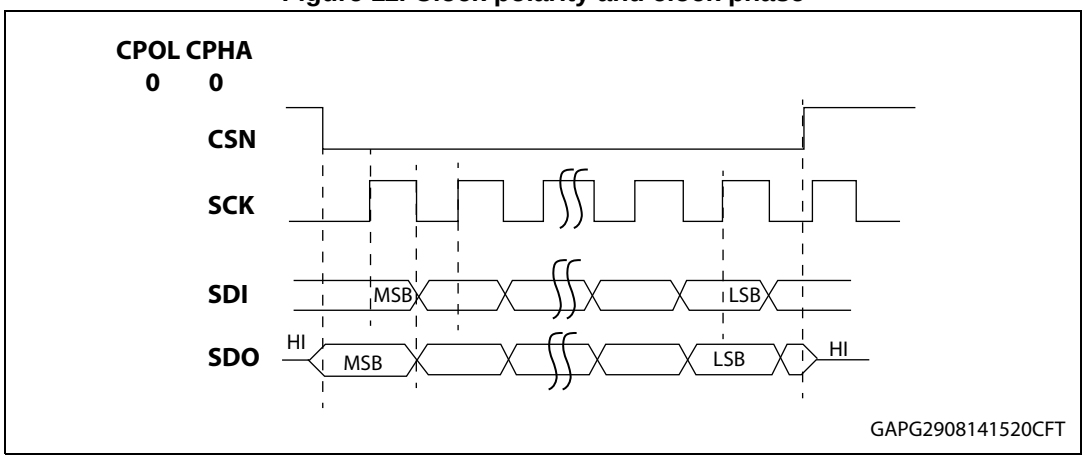
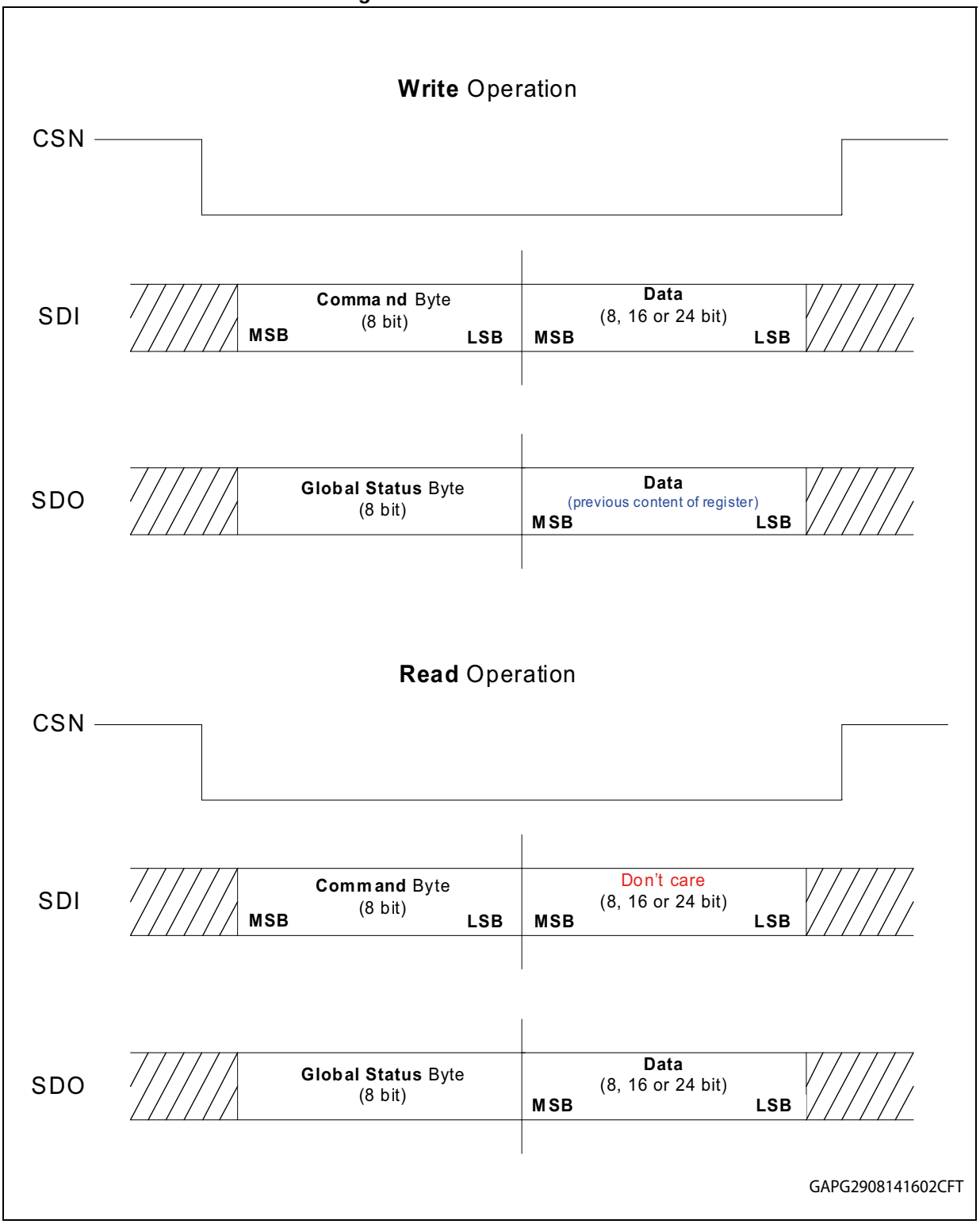


Figure 12. SPI frame structure



8.2 SPI communication flow

8.2.1 General description

The proposed SPI communication is based on a standard SPI interface structure using CSN (chip select not), SDI (serial data in), SDO (serial data out/error) and SCK (serial clock) signal lines.
At the beginning of each communication the master reads the <*SPI-frame-ID*> register (ROM address 3EH) of the slave device. This 8-bit register indicates the SPI frame length (16 bit for the L99MC6GJ) and the availability of additional features.
Each communication frame consists of an instruction byte which is followed by 1 data byte (see *Figure 12*).
The data returned on SDO within the same frame always starts with the <Global Status> register. It provides general status information about the device. It is followed by 1 byte (that is 'In-frame-response', see *Figure 12*).

For Write cycles the <*Global Status*> register is followed by the previous content of the addressed register.
For Read cycles the <Global Status> register is followed by the content of the addressed register.

Table 12. Command byte - general description

MSB							**LSB**
Operating code		Address					
OC1	OC0	A5	A4	A3	A2	A1	A0

Table 13. Data byte - general description

MSB							**LSB**
Bit7	Bit6	Bit5	Bi4	Bit3	Bit2	Bit1	Bit0

8.2.2 Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Read>, <Write>, <Read and Clear Status>, <Read Device Information>) and a 6-bit address.

Table 14. Command byte

MSB							**LSB**
Operating code		Address					
OC1	OC0	A5	A4	A3	A2	A1	A0

Operating code definition

Table 15. Operating code definition

OC1	OC0	Meaning
0	0	<Write mode>
0	1	<Read mode>
1	0	<Read and Clear Status>
1	1	<Read Device Information>

The <Write mode> and <Read mode> operations allow access to the RAM of the device, that is write to control registers or read status information.

A <Read and Clear Status> operation addressed to a device specific status register reads back and subsequently clear this status register. A <Read and Clear Status> operation with address 3FH clears all status registers at a time.

A <Read and Clear Status> operation addressed to an unused RAM address or configuration register address is identical to a <Read mode> operation (in case of unused RAM address, the second byte is equal to 00H).

<Read Device Information> allows access to the ROM area which contains device related information such as the product family, product name, silicon version and register width.

8.2.3 Global status register

Table 16. Global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global error flag (GEF)	Communication error	Chip reset	TSD Chip overload	Temperature warning	Open-load detected	Overcurrent detected	Unused

Table 17. Global status register description

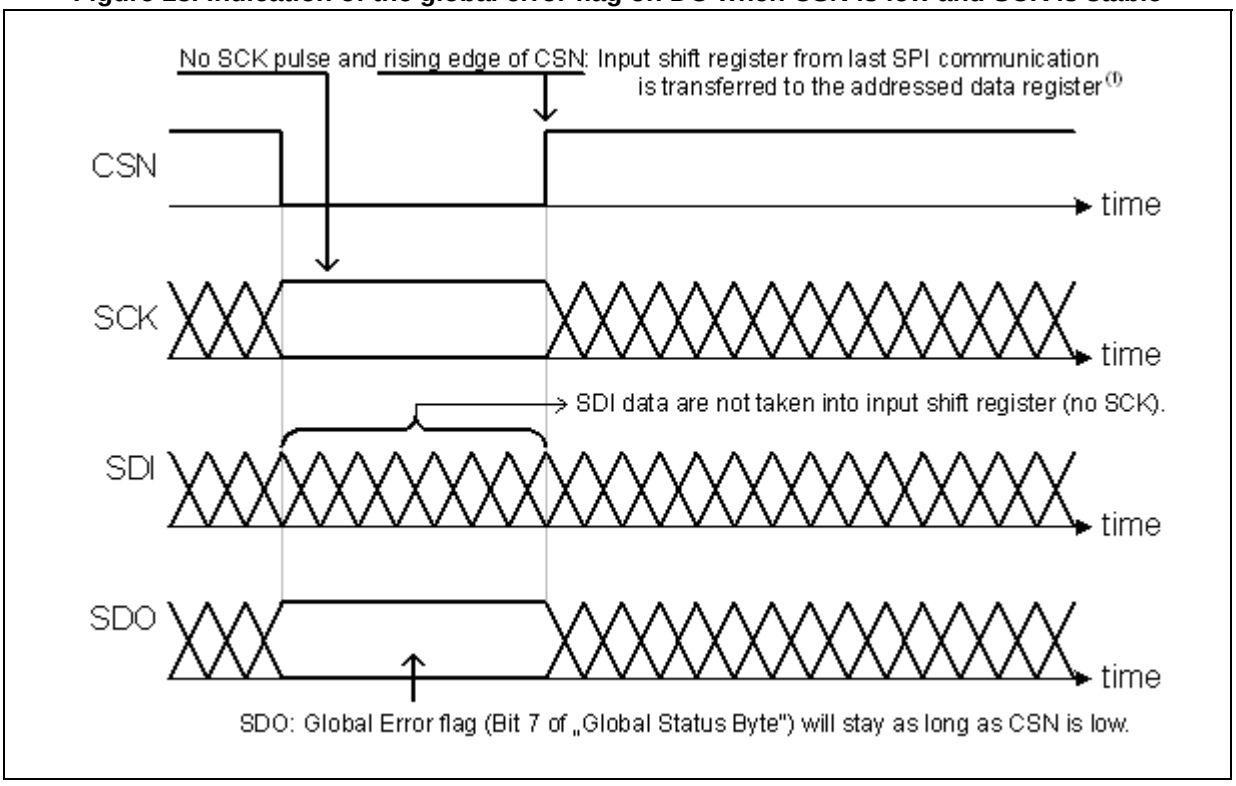
Bit	Description	Polarity	Comment
0	Unused	Active high	Always returns ‘0’
1	Overcurrent detected	Active high	Set by any overcurrent event
2	Open-load detected	Active high	Set by any open-load event
3	Temperature warning	Active high	-
4	Thermal shutdown / chip overload	Active high	-
5	Chip reset	Active low	Activated by all internal reset events that change device state or configuration registers (for example software reset, V_{CC} undervoltage, etc.). The bit is cleared after a valid communication with any register. This bit is initially ‘0’ and is set to ‘1’ by a valid SPI communication

Table 17. Global status register description (continued)

Bit	Description	Polarity	Comment
6	Communication error	Active high	Bit is set if the number of clock cycles during CSN = low does not match with the specified frame width or if an invalid bus condition is detected (DI always 1). DI always 0 automatically leads to clearing the enable bit in CTRL0 and is not signaled as communication error.
7	Global Error flag	Active high	Logic OR combination of all failures in the <Global Status Byte>.

The <*Global Error Flag*> is generated by an OR-combination of all failure events of the device (that is <*Global Status Register*>, *[0:6]*).

Figure 13. Indication of the global error flag on DO when CSN is low and SCK is stable



1. The last transferred SPI command is still valid in the input shift register. If SCK is stable (high or low) during a CSN low pulse, at the rising edge of CSN the last transferred SPI command is still valid in the input shift register and is repeated. Therefore, it is recommended to send a complete SPI frame to monitor the status of the L99MC6GJ.

Writing to the selected data input register is only enabled if exactly one frame length is transmitted within one communication frame (that is CSN low). If more or less clock pulses are counted within one frame, the complete frame is ignored and a SPI frame error is signaled in the Global Status register. This safety function is implemented to avoid an unwanted activation of output stages by a wrong communication frame.

For Read operations, the <*communication error*> bit in the <*Global Status Register*> is set, but the register to be read is still transferred to the DO pin. If the number of clock cycles is smaller than the frame width, the data at DO is truncated. If the number of clock cycles is larger than the frame width, the data at DO is filled with ‘0’ bits.

Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

Note: If the frame width is greater than 16 bits, initial Read of <SPI-frame-ID> using a 16-bit communication sets the <communication Error bit> of the <Global Status> register. A subsequent correct length transaction is necessary to correct this bit.

8.3 Write operation

OC0, OC1: operating code (00 for ‘Write’ mode)

Table 18. Command byte for Write mode

MSB							**LSB**
Operating code		Address					
0	0	A5	A4	A3	A2	A1	A0

The Write operation starts with a command byte followed by 1 data byte.
For Write cycles the <*Global Status*> register is followed by the previous content of the addressed register.
The RAM memory area consists of 8-bit registers. All unused RAM addresses are read as ‘0’.

Failures are indicated by activating the corresponding bit of the <Global Status> register.

Note: The register definition for RAM address 00H is device specific.
A register value of all 0 causes a device reset (interpreted as ‘Data-in short to GND’).

8.4 Read operation

OC0, OC1: operating code (01 for ‘Read’ mode)

Table 19. Command byte for Read mode

MSB							**LSB**
Operating code		Address					
0	1	A5	A4	A3	A2	A1	A0

The Read operation starts with a command byte followed by 1 data byte. The content of the data byte is ‘do not care’. The content of the addressed register is shifted out at SDO within the same frame (‘in-frame response’).

The returned data byte represents the content of the register to be read.

Failures are indicated by activating the corresponding bit of the <Global Status> register.

8.5 Read and Clear Status operation

OC0, OC1: operating code (10 for ‘Read and Clear Status’ mode)

Table 20. Command byte for Read and Clear Status operation

MSB							LSB
Operating code		Address					
1	0	A5	A4	A3	A2	A1	A0

The ‘Read and Clear Status’ operation starts with a command byte followed by 1 data byte. The content of the data byte is ‘do not care’. The content of the addressed status register is transferred to SDO within the same frame (‘in-frame response’) and is subsequently cleared.

A <Read and Clear Status> operation with address 3FH clears all status registers simultaneously.

A <Read and Clear Status> operation addressed to an unused RAM address or to the configuration register (3FH) is identical to a <Read mode> operation (in case of unused RAM address, the second byte is equal to 00H).

The returned data byte represents the content of the register to be read.
Failures are indicated by activating the corresponding bit of the <Global Status> register.

8.6 Read Device Information

OC0, OC1: operating code (11 for ‘Read Device Information’ mode)

Table 21. Command byte for Read Device Information

MSB							LSB
Operating code		Address					
1	1	A5	A4	A3	A2	A1	A0

The device information is stored at the ROM. In the ROM memory area, the first 8 bits are used.
All unused ROM addresses is read as ‘0’.

Note: ROM address 3FH is unused. An attempt to access this address is recognized as a communication line error (‘Data-in stuck to V_{CC}’) and the standby mode is automatically entered (all internal registers are cleared).

9 SPI control and status register

9.1 RAM memory map

Table 22. RAM memory map

Address	Name	Access	Content
00h	CTRL 0	Read/Write	Global enable, channels 3 and 6 control register
01h	CTRL 1	Read/Write	CP, channels 2 and 5 control register
02h	CTRL 2	Read/Write	CP, channels 1 and 4 control register
03h	Unused	-	-
04h	STAT 0	Read only	Open-load / thermal status register
05h	STAT 1	Read only	Overcurrent / thermal status register

9.2 ROM memory map (access with OC0 and OC1 set to ‘1’)

Table 23. ROM memory map

Address	Name	Access	Content
00h	ID Header	Read only	42h (device class ASSP, 2 additional information bytes)
01h	Product ID	Read only	06H
02h	Category / Version	Read only	18h (multi channel driver, last 3 LSB = 0: engineering samples)
3Eh	SPI-Frame ID	Read only	01h (no burst mode, no watchdog, 16 bit frame SPI)

9.3 Control and status registers

Table 24. Control register 0

Adress	Access	Data Byte							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Global enable, Channel 3&6 control							
00h	R/W	EN	CH6 [2]	CH6 [1]	CH6 [0]	Bridge 3&6	CH3 [2]	CH3 [1]	CH3 [0]
Default		0	0	0	0	0	0	0	0

Table 25. Control register 1

Adress	Access	Data Byte							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Channel 2&5 control							
01h	R/W	ENCP	CH5 [2]	CH5 [1]	CH5 [0]	Bridge 2&5	CH2 [2]	CH2 [1]	CH2 [0]
Default		1	0	0	0	0	0	0	0

Table 26. Control register 2

Adress	Access	Data Byte							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Channel 1&4 control							
02h	R/W	DISCP	CH4 [2]	CH4 [1]	CH4 [0]	Bridge 1&4	CH1 [2]	CH1 [1]	CH1 [0]
Default		0	0	0	0	0	0	0	0

Table 27. Status register 0

Adress	Access	Data Byte							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Open-load, thermal status							
04h	R	TSD	TWARN	OL CH6	OL CH5	OL CH4	OL CH3	OL CH2	OL CH1

Table 28. Status register 1

Adress	Access	Data Byte							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Overcurrent, thermal status							
05h	R	TSD	TWARN	OC CH6	OC CH5	OC CH4	OC CH3	OC CH2	OC CH1

9.3.1 Channel configuration decoding

Table 29. Channel configuration decoding

CHx [2]	CHx [1]	CHx [0]	CHx	PWM mode	Overcurrent recovery	Slew Rate	Open-load detection
0	0	0	Off(1)	No	-	High	Off
1	1	1	Off(1)	No	-	Low	On

Table 29. Channel configuration decoding (continued)

CHx [2]	CHx [1]	CHx [0]	CHx	PWM mode	Overcurrent recovery	Slew Rate	Open-load detection
0	0	1	On	No	No	High	-
0	1	0	On	No	No	Low	-
0	1	1	On	No	Yes	Low	-
1	0	1	IN/PWM(2)	Yes	No	High	Off
1	1	0	IN/PWM(2)	Yes	No	Low	On

1. The state of the channel 2 is according to the IN/PWM signal
2. The output state is according to the IN/PWM signal, note that bridge mode and PWM mode may not be activated at the same time for channels 2 and 5.

9.3.2 Register description

Table 30. Register description

Name	Comment
EN	Global device enable bit. If this bit is reset, the device goes in standby mode.
CHx [2:0]	Channel output configuration (see *Table 29*). Note that channel 2 is directly driven by the external IN/PWM pin and thus can not be configured independently from the PWM configuration of other channels.
Bridge	Activate Bridge mode between channels 3 and 6, channels 2 and 5, channels 1 and 4. Any polarity change is delayed by masking time of cross conduction protection If wrong SPI commands try to turn on the channels 3 and 6, channels 2 and 5, channels 1 and 4 simultaneously, the high-side (channels 3, 2, 1) has the priority whereas channels 6, 5, 4 is (or stay) deactivated.
ENCP	This bit is preset to ‘1’ at startup. To deactivate the internal charge pump ENCP has to be reset together with setting DISCP (CTRL 2). This mechanism avoids unwanted charge pump deactivation after an undetected communication error. It is recommended to check the state of the charge pump deactivation bits at every access of CTRL 1 and CTRL 2.
DISCP	This bit is reset to ‘0’ at startup. To deactivate the internal charge pump DISCP has to be set together with resetting ENCP (CTRL 1)
TSD	Overtemperature detected: all the drivers are shutdown
TWARN	Overtemperature warning level detected, information only
OL [6:1]	Open-load error detected, information only
OC [6:1]	Overcurrent error detected, drivers are deactivated and re-enabled cyclically when bulb mode is configured. Note: in order to detect a real overload condition, the application software must make sure, that the corresponding OC bit remains cleared after a maximum heat up time of the load.

Note: Every output stage is protected against overtemperature and overcurrent. While still configured as ON, the output stage can be deactivated by the corresponding error bits in the status registers. In order to reactivate the drivers, the status registers have to be cleared by a specific SPI command.

9.4 Examples

9.4.1 Example 1:Switch on channel 1

It is assumed that the charge pump is already activated (ENCP1 = 1 and DISCP2 = 0, POR default)

Table 31. Command byte - example 1

MSB							LSB
Operating code		Address					
0	0	0	0	0	0	1	0

Table 32. Data byte - example 1

MSB							LSB
0	0	0	0	0	0	0	1

From *Table 31* and *Table 32* follow that the value 01h is written at RAM address 02h (control register 2).

Table 33 describe more in detail the data byte structure.

Table 33. Data byte description - example 1

DISCP	CH4 [2]	CH4 [1]	CH4 [0]	Bridge 1&4	CH1 [2]	CH1 [1]	CH1 [0]
0	0	0	0	0	0	0	1

Hereafter the actions linked to each value of bit or group of bits:

- **DISCP = 0**: Charge pump stays activated
- **CH4[2:0] = 000b**: Channel 4 is off, open-load detection in off-state disabled
- **BRIDGE_1&4 = 0**: Bridge mode disabled
- **CH4[2:0] = 001b**: Channel 1 is on, high slew rate, PWM not activated, overcurrent recovery deactivated.

9.4.2 Example 2: Bridge mode configuration

Table 34. Command byte 1 - example 2

MSB							LSB
Operating code		Address					
0	0	0	0	0	0	0	1

Table 35. Data byte 1 - example 2

MSB							LSB
1	0	1	0	1	0	0	0

From *Table 34* and *Table 35* follow that the value A8h is written at RAM address 01h (control register 1).

Table 36 describe more in detail the data byte structure.

Table 36. Data byte description 1 - example 2

ENCP	CH5 [2]	CH5 [1]	CH5 [0]	Bridge 2&5	CH2 [2]	CH2 [1]	CH2 [0]
1	0	1	0	1	0	0	0

Hereafter the actions linked to each value of bit or group of bits:

- **ENCP = 1**: Charge pump stays activated
- **CH5[2:0] = 010b**: Channel 5 is on, PWM disabled, overcurrent recovery mode disabled, low slew rate
- **BRIDGE_2&5 = 1**: Bridge mode for channel 2 and channel 5 activated
- **CH2[2:0] = 000b**: Channel 2 is off, open-load detection in off-state disabled

Table 37. Command byte 2 - example 2

MSB							LSB
Operating code		Address					
0	0	0	0	0	0	1	0

Table 38. Data byte 2 - example 2

MSB							LSB
0	0	0	0	1	0	1	0

From *Table 37* and *Table 38* follow that the value 0Ah is written at RAM address 02h (control register 2).

Table 39 describe more in detail the data byte structure.

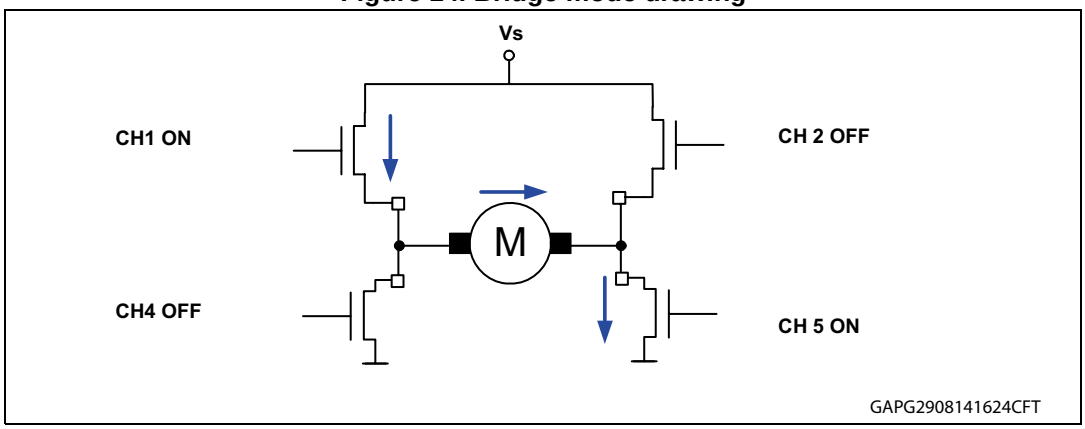
Table 39. Data byte description 2 - example 2

DISCP	CH4 [2]	CH4 [1]	CH4 [0]	Bridge 1&4	CH1 [2]	CH1 [1]	CH1 [0]
0	0	0	0	1	0	1	0

Hereafter the actions linked to each value of bit or group of bits:

- **DISCP = 0**: Charge pump stays activated
- **CH4[2:0] = 000b**: Channel 4 is off, open-load detection in off-state disabled
- **BRIDGE_1&4 = 1**: Bridge mode for channel 1 and channel 4 activated
- **CH4[2:0] = 010b**: Channel 1 is on, PWM disabled, overcurrent recovery mode disabled, low slew rate

Figure 14. Bridge mode drawing



9.4.3 Example 3: Open-load detection in off-state in bridge configuration

Table 40. Command byte 1 - example 3

MSB							LSB
Operating code		Address					
0	0	0	0	0	0	0	1

Table 41. Data byte 1 - example 3

MSB							LSB
1	1	1	1	1	0	0	0

From *Table 40* and *Table 41* follow that the value F8h is written at RAM address 01h (control register 1).

Table 42 describe more in detail the data byte structure.

Table 42. Data byte description 1 - example 3

ENCP	CH5 [2]	CH5 [1]	CH5 [0]	Bridge 2&5	CH2 [2]	CH2 [1]	CH2 [0]
1	1	1	1	1	0	0	0

Hereafter the actions linked to each value of bit or group of bits:

- **ENCP = 1**: Charge pump stays activated
- **CH5[2:0] = 111b**: Channel 5 is off, open-load detection in off-state enabled
- **BRIDGE_2&5 = 1**: Bridge mode for channel 2 and channel 5 activated
- **CH2[2:0] = 000b**: Channel 2 is off, open-load detection in off-state disabled

Table 43. Command byte 2 - example 3

MSB							LSB
Operating code		Address					
0	0	0	0	0	0	1	0

Table 44. Data byte 2 - example 3

MSB							LSB
0	0	0	0	1	0	1	0

From *Table 43* and *Table 44* follow that the value 0Ah is written at RAM address 02h (control register 2).

Table 45 describe more in detail the data byte structure.

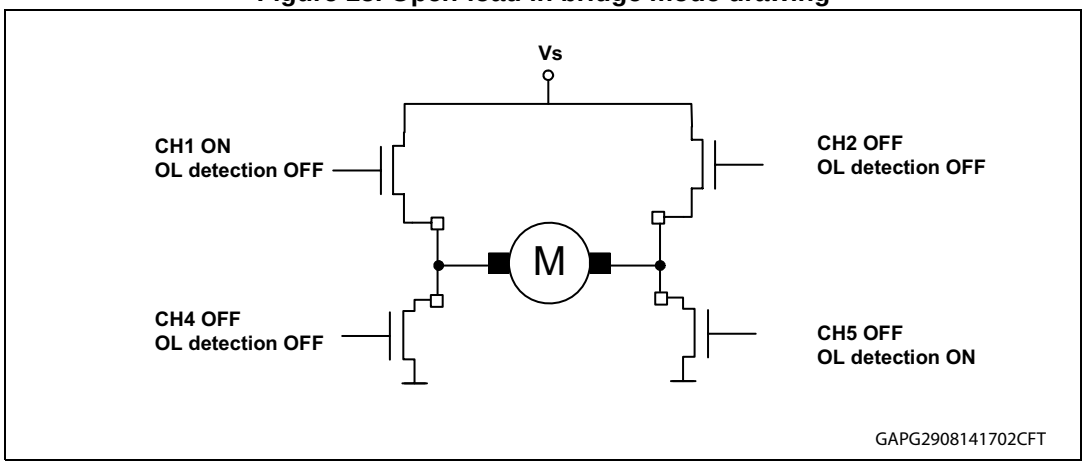
Table 45. Data byte description 2 - example 3

DISCP	CH4 [2]	CH4 [1]	CH4 [0]	Bridge 1&4	CH1 [2]	CH1 [1]	CH1 [0]
0	0	0	0	1	0	1	0

Hereafter the actions linked to each value of bit or group of bits:

- **DISCP = 0**: Charge pump stays activated
- **CH4[2:0] = 000b**: Channel 4 is off, open-load detection in off-state disabled
- **BRIDGE_1&4 = 1**: Bridge mode for channel 1 and channel 4 activated
- **CH1[2:0] = 010b**: Channel 1 is on, PWM disabled, overcurrent recovery mode disabled, low slew rate

Figure 15. Open-load in bridge mode drawing

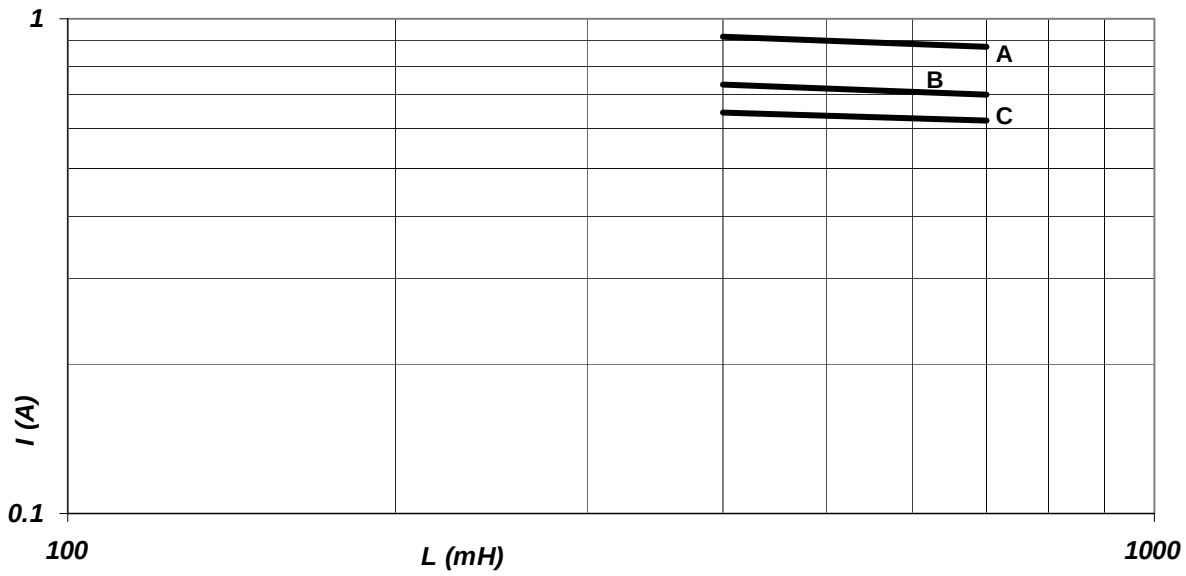


There are two operating conditions:

- **Case 1:** The motor is connected, drain of channel 5 is pulled up by channel 1 (on) through the motor, then no open-load detected on channel 5
- **Case 2**: The motor is not connected and the drain voltage of channel 5 is below the open-load threshold, then open-load detected on channel 5

10 Maximum demagnetization energy

Figure 16. Configurable switch HSD - maximum turn-off current versus inductance

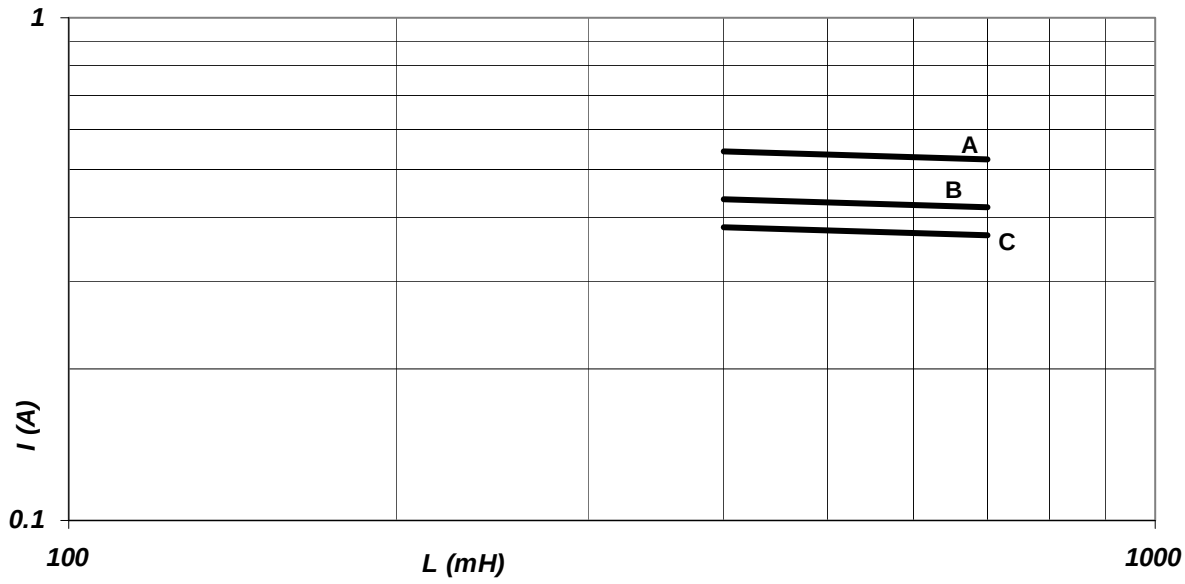


A: Single pulse, T_j = 150 °C

B: Repetitive pulse, T_j = 100 °C

C: Repetitive pulse, T_j = 125 °C

Figure 17. Configurable switch LSD - maximum turn-off current versus inductance

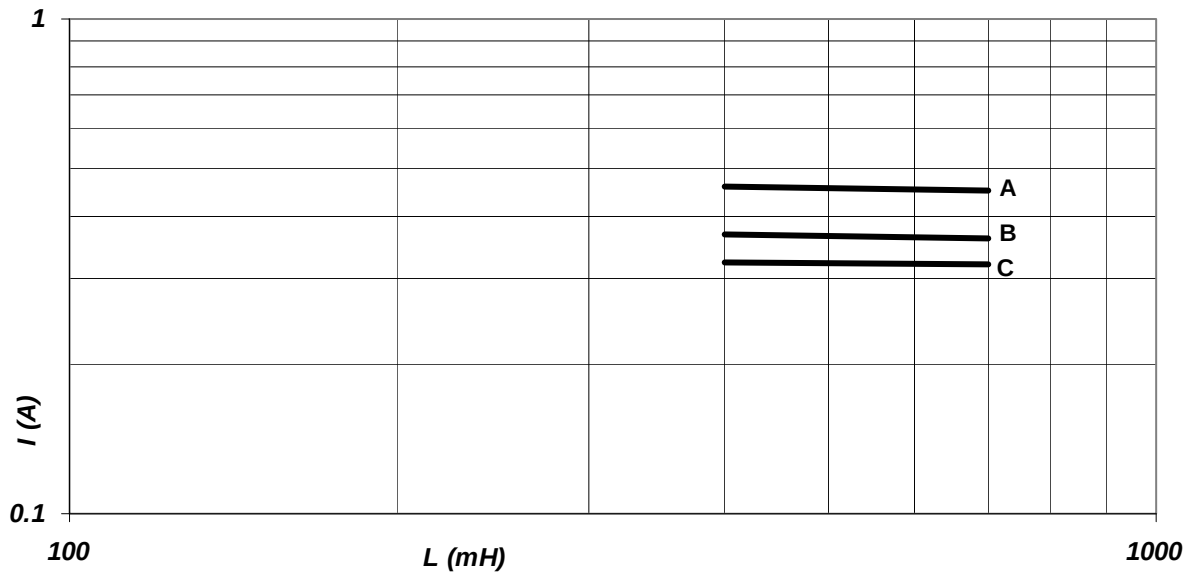


A: Single pulse, T_j = 150 °C

B: Repetitive pulse, T_j = 100 °C

C: Repetitive pulse, T_j = 125 °C

Figure 18. Fixed LSD switch - maximum turn-off current versus inductance



A: Single pulse, T_j = 150 °C

B: Repetitive pulse, T_j = 100 °C

C: Repetitive pulse, T_j = 125 °C

11 Application examples

Figure 19. L99MC6GJ as driver for incandescent bulb, LEDs and high-side or low-side relays

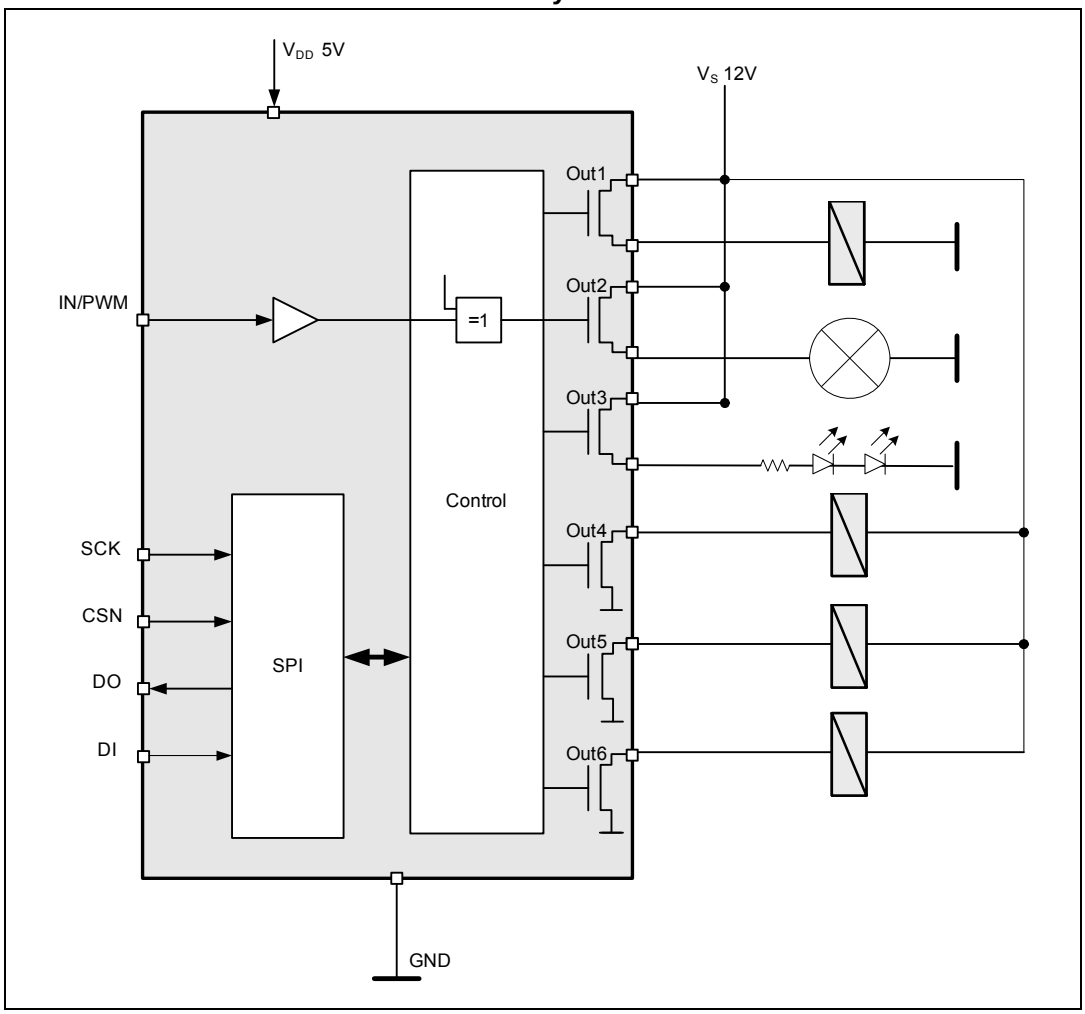


Figure 20. L99MC6GJ as motor driver (for example, for mirror adjustment)

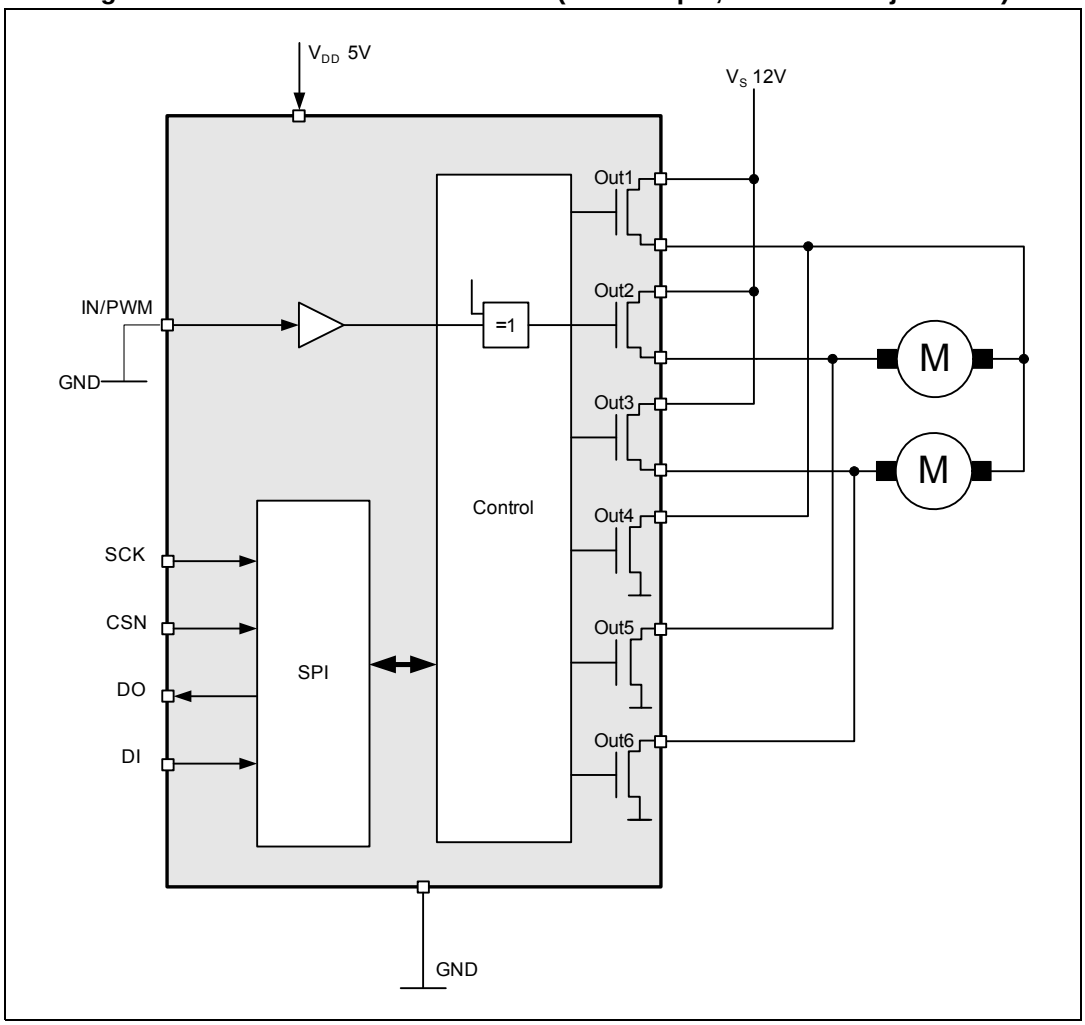
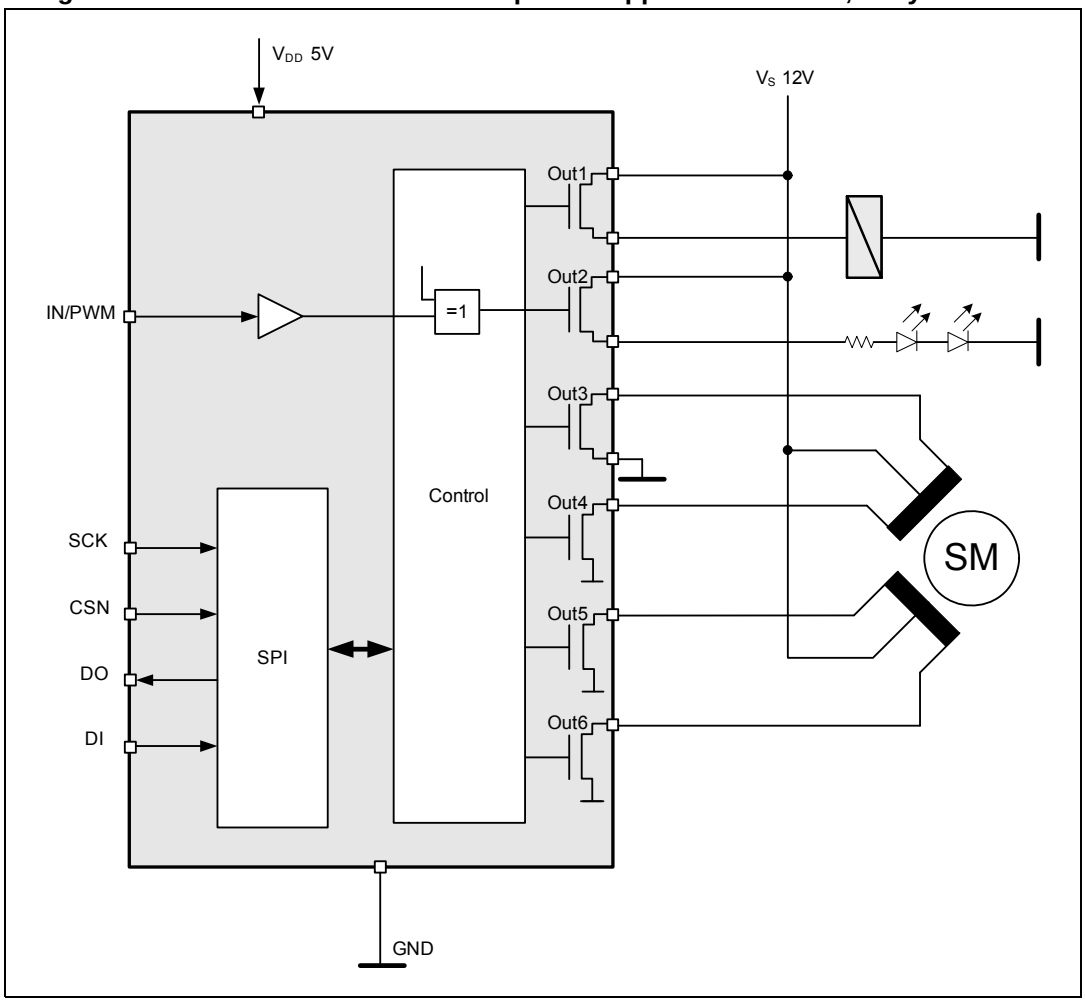


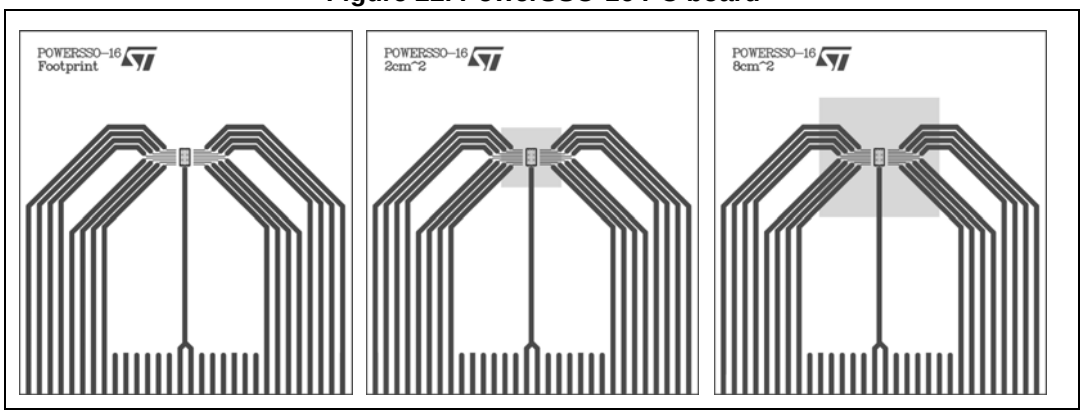
Figure 21. L99MC6GJ as driver for unipolar stepper motor driver, relay and LEDs



12 Package and PCB thermal data

12.1 PowerSSO-16 thermal data

Figure 22. PowerSSO-16 PC board



Note: Layout condition of thermal resistance measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness =1.6 mm, Cu thickness = 70 µm (front and back side) thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 25 µm, footprint dimension 2.5 mm x 4.2 mm).

Table 46. Auto and mutual thermal resistance - footprint

	HSD 1	HSD 2	HSD 3	LSD 4	LSD 5	LSD 6
HSD 1	89.57	85.83	84.41	88.89	87.06	85.84
HSD 2	85.83	89.57	84.41	87.06	88.89	87.06
HSD 3	84.41	84.41	89.57	85.84	87.06	88.89
LSD 4	88.89	87.06	85.84	93.58	90.54	89.08
LSD 5	87.06	88.89	87.06	90.54	93.58	90.54
LSD 5	85.84	87.06	88.89	89.08	90.54	93.58

Table 47. Auto and mutual thermal resistance - 2 cm^2 of Cu heatsink

	HSD 1	HSD 2	HSD 3	LSD 4	LSD 5	LSD 6
HSD 1	59.96	55.06	54.23	58.25	56.08	54.71
HSD 2	55.06	59.96	54.23	56.08	58.25	56.08
HSD 3	54.23	54.23	59.96	54.71	56.08	58.25
LSD 4	58.25	56.08	54.71	61.80	60.37	59.45
LSD 5	56.08	58.25	56.08	60.37	61.80	60.37
LSD 5	54.71	56.08	58.25	59.45	60.37	61.80

Table 48. Auto and mutual thermal resistance - 8 cm^2 of Cu heatsink

	HSD 1	HSD 2	HSD 3	LSD 4	LSD 5	LSD 6
HSD 1	46.51	43.16	41.49	45.19	43.06	42.08
HSD 2	43.16	46.51	41.49	43.06	45.19	43.06
HSD 3	41.49	41.49	46.51	42.08	43.06	45.19
LSD 4	45.19	43.06	42.08	47.19	46.31	45.19
LSD 5	43.06	45.19	43.06	46.31	47.19	46.31
LSD 5	42.08	43.06	45.19	45.19	46.31	47.19

Equation 1 represents $\Delta T_{j\text{-}amb}$ calculation of a full loaded device for the HSD1 junction.

Equation 1

$$\Delta T_{HSD1} = Rth_{HSD1} * Pd_{HSD1} + Rth_{HSD1,HSD2} * Pd_{HSD2} + Rth_{HSD1,HSD3} * Pd_{HSD3} + \\ + Rth_{HSD1,LSD4} * Pd_{LSD4} + Rth_{HSD1,LSD5} * Pd_{LSD5} + Rth_{HSD1,LSD6} * Pd_{LSD6}$$

13 Package and packing information

13.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

13.2 PowerSSO-16 package information

Figure 23. PowerSSO-16 package dimensions

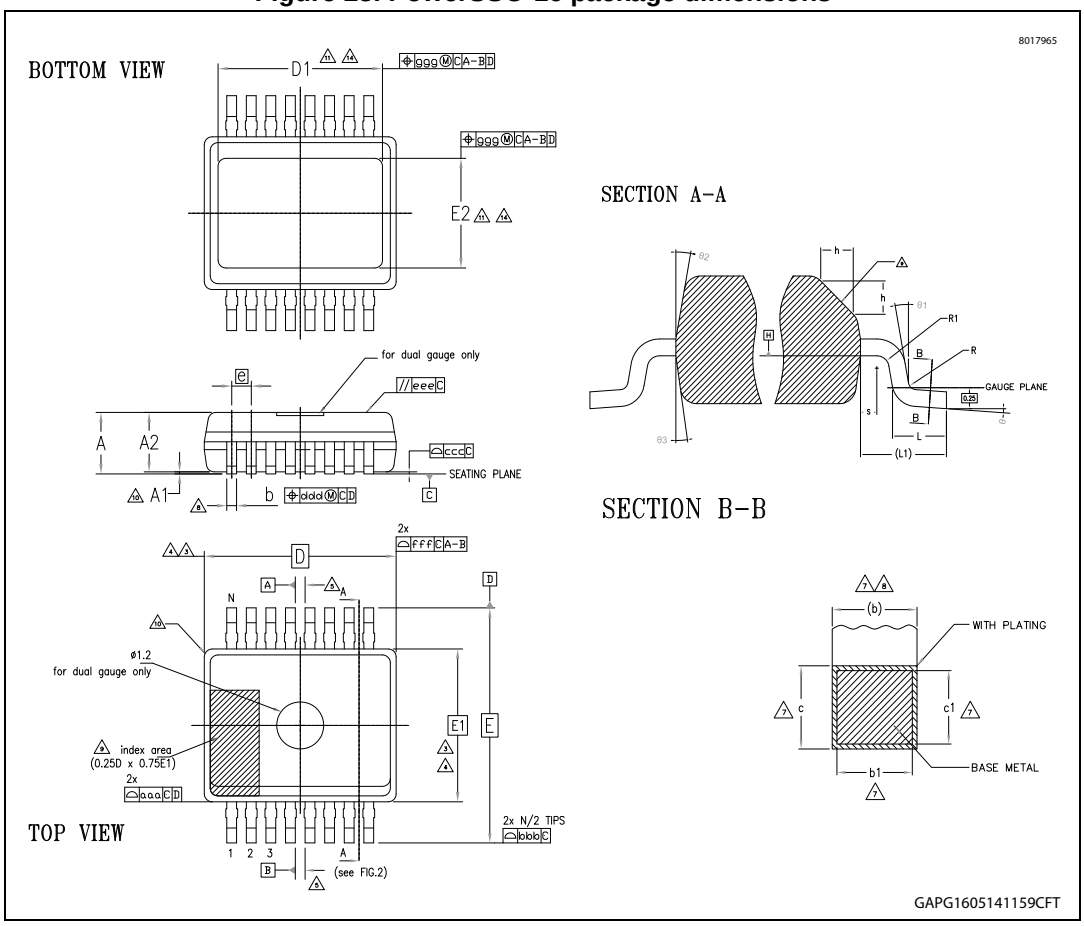
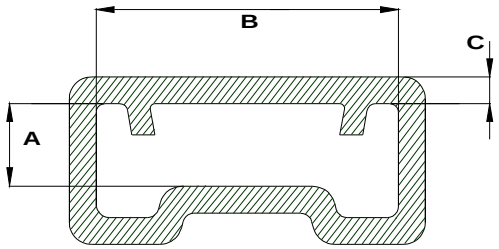


Table 49. PowerSSO-16 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
Θ1	0°		
Θ2	5°		15°
Θ3	5°		15°
A			1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.20		0.30
b1	0.20	0.25	0.28
c	0.19		0.25
c1	0.19	0.20	0.23
D	4.90 BSC		
D1	3.60		4.20
e	0.50 BSC		
E	6.00 BSC		
E1	3.90 BSC		
E2	1.90		2.50
h	0.25		0.50
L	0.40	0.60	0.85
L1	1.00 REF		
N	16		
R	0.07		
R1	0.07		
S	0.20		
Tolerance of form and position			
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.08		
eee	0.10		
fff	0.10		
ggg	0.15		

13.3 Packing information

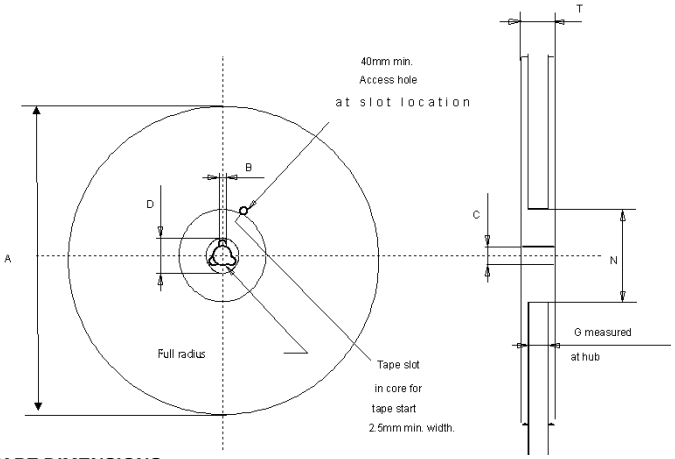
Figure 24. PowerSSO-16 tube shipment (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

Figure 25. PowerSSO-16 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

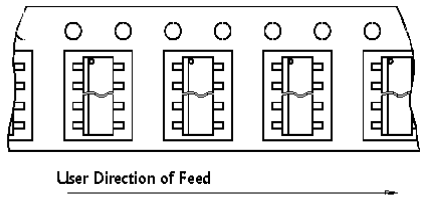
Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

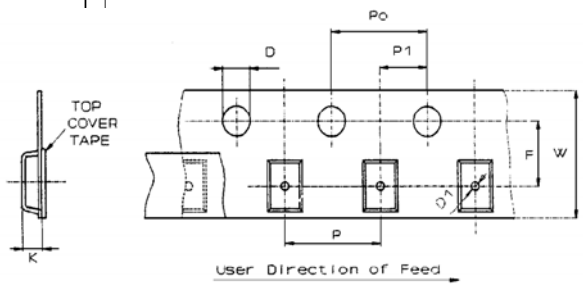
TAPE DIMENSIONS

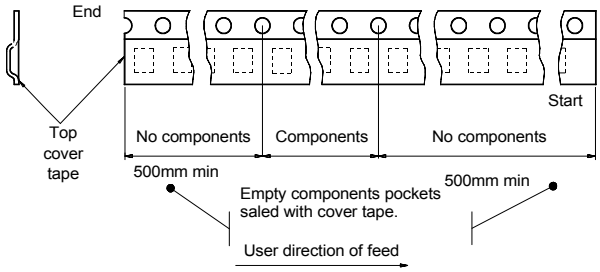
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	12
Tape hole spacing	**P0 (± 0.1)**	4
Component spacing	**P**	8
Hole diameter	**D (± 0.05)**	1.5
Hole diameter	**D1 (min)**	1.5
Hole position	**F (± 0.1)**	5.5
Compartment depth	**K (max)**	4.5
Hole spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







Appendix A Acronyms

Table 50. Acronyms

Acronym	Name
CSN	Chip select not
CTRL	Control register
POR	Power-on reset
SCK	Serial clock
SDI	Serial data input
SDO	Serial data output
SPI	Serial peripheral interface
SR	Slew rate
STAT	Status register

Revision history

Table 51. Document revision history

Date	Revision	Changes
14-Jan-2015	1	Initial release.
25-Mar-2015	2	Updated *Table 1: Device summary*
21-Nov-2016	3	Added AEC-Q100 qualified in *Features*. Updated *Table 4: ESD protection*