

ESD protection for high-speed interfaces

31 July 2018

Product data sheet

1. General description

The device is designed to protect high-speed interfaces such as USB 2.0 ports against ElectroStatic Discharge (ESD).

The device includes four high-level ESD protection diode structures for high-speed signal lines. It is encapsulated in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of 0.85 pF maximum. This configuration provides protection to downstream components from ESD voltages up to ±12 kV contact according to IEC 61000-4-2, level 4.

2. Features and benefits

- System ESD protection for USB 2.0
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±12 kV according to IEC 61000-4-2, level 4
- Line capacitance of 0.85 pF maximum for each channel

3. Applications

The device is designed for receiver and transmitter port protection in:

- Portable devices
- TVs, monitors
- DVD recorders and players
- Notebooks, mother boards, graphic cards and ports
- Set-top boxes and game consoles



ESD protection for high-speed interfaces

4. Pinning information

Table 1. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	LINE1	line 1 ESD protection for I/O signals	<u> </u>	1 3 4 6
2	GND	ground	0	本 本 本 本
3	LINE3	line 3 ESD protection for I/O signals	☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐	***
4	LINE4	line 4 ESD protection for I/O signals		2 018aaa176
5	n.c	not connected		
6	LINE6	line 6 ESD protection for I/O signals		

5. Ordering information

Table 2. Ordering information

Type number	Package				
	Name	Description	Version		
IP4285CZ6-TD	TSOP6	plastic, surface-mounted package (SC-74)	SOT457		

6. Marking

Table 3. Marking codes

Type number	Marking code
IP4285CZ6-TD	85

ESD protection for high-speed interfaces

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _I	input voltage			-0.5	5.5	V
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; contact discharge	[1]	-12	12	kV
		IEC 61000-4-2, level 4; air discharge	[1]	-15	15	kV
T _{stg}	storage temperature			-55	125	°C
T _{amb}	ambient temperature			-40	85	°C

^[1] Pins 1, 3, 4 and 6 to ground.

8. Characteristics

Table 5. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{BR}	breakdown voltage	I _I = 1 mA; T _{amb} = 25 °C		6	-	9	V
I _{LR}	reverse leakage current	per channel; V _I = 5 V; T _{amb} = 25 °C		-	-	1	μΑ
V _F	forward voltage	I _I = 1 mA; T _{amb} = 25 °C		-	0.7	-	V
C _{line}	line capacitance	f = 1 MHz; V _I = 0 V; T _{amb} = 25 °C	[1]	-	-	0.85	pF
		f = 1 MHz; V _I = 2.5 V; T _{amb} = 25 °C	[1]	-	-	0.75	pF
ΔC_{line}	line capacitance difference		[1]	-	-	0.1	pF
r _{dyn}	dynamic resistance	Surge, positive transient; T _{amb} = 25 °C	[2]	-	0.42	-	Ω
		Surge, negative transient; T _{amb} = 25 °C	[2]	-	0.33	-	Ω
		TLP, positive transient; T _{amb} = 25 °C	[3]	-	0.42	-	Ω
		TLP, negative transient; T _{amb} = 25 °C	[3]	-	0.33	-	Ω
V _{CL}	clamping voltage	I_{PP} = 4 A; positive transient; T_{amb} = 25 °C	[2]	-	4	-	V
		I _{PP} = 4 A; negative transient; T _{amb} = 25 °C	[2]	-	-2.3	-	V

^[1] The parameter is guaranteed by design.

^[2] According to IEC 61000-4-5 (8/20 µs current waveform).

^{[3] 100} ns Transmission Line Pulse (TLP), 50 Ω , pulser at 80 ns.

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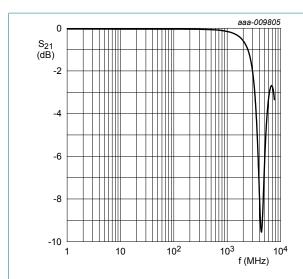


Fig. 1. Insertion loss; typical values

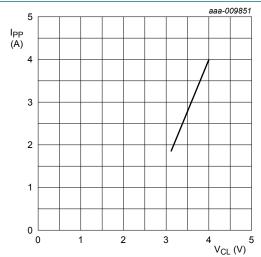


Fig. 3. Dynamic resistance with positive clamping; typical values

IEC 61000-4-5; t_p = 8/20 µs; positive pulse

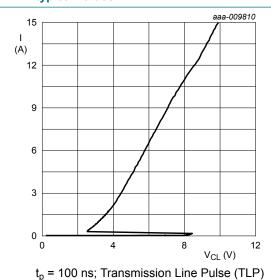


Fig. 5. Dynamic resistance with positive clamping; typical values

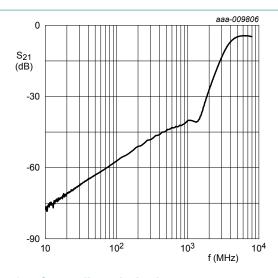


Fig. 2. Crosstalk; typical values

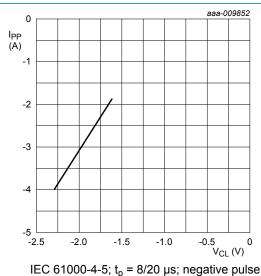
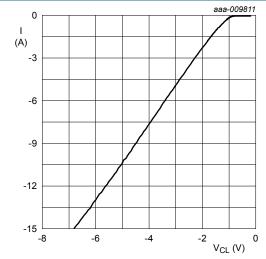


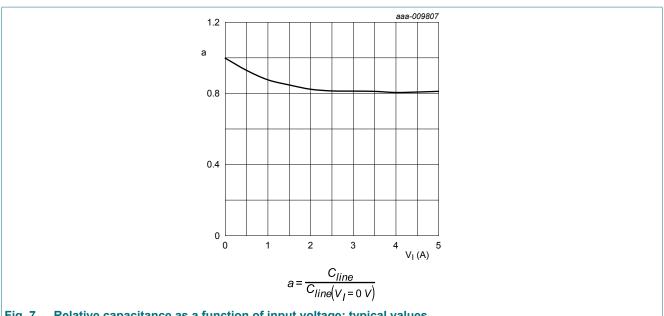
Fig. 4. Dynamic resistance with negative clamping; typical values



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig. 6. Dynamic resistance with negative clamping; typical values

ESD protection for high-speed interfaces

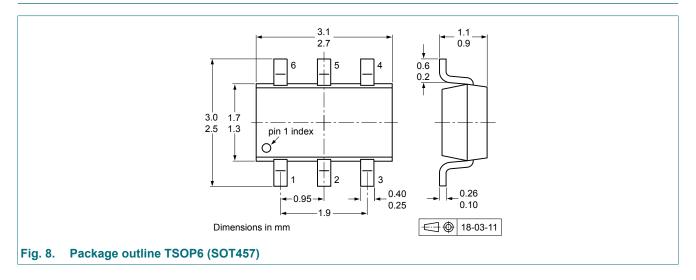


ESD protection for high-speed interfaces

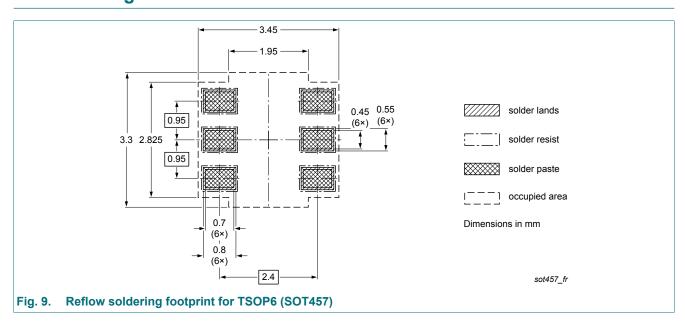
9. Application information

The device uses an advanced clamping structure, which shows a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in the snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

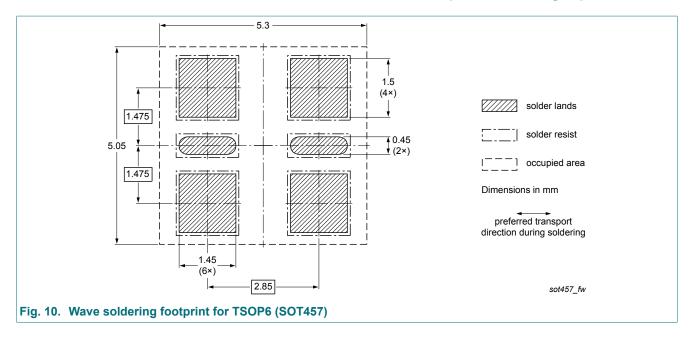
10. Package outline



11. Soldering



ESD protection for high-speed interfaces



ESD protection for high-speed interfaces

12. Revision history

Table 6. Revision history

Table 0. Revision history							
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
IP4285CZ6-TD v.5	20180731	Product data sheet	-	IP4285CZ6-TD v.4			
Modifications	Nexperia.	ata sheet has been redesignen adapted to the new com	. •	, ,			
IP4285CZ6-TD v.4	20140321	Product data sheet	-	IP4285CZ6-TD v.3			
IP4285CZ6-TD v.3	20121108	Product data sheet	-	IP4285CZ6-TD v.2			
IP4285CZ6-TD v.2	20111209	Preliminary data sheet	-	IP4285CZ6-TD v.1			
IP4285CZ6-TD v.1	20111202	Objective data sheet	-	-			

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13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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ESD protection for high-speed interfaces

Contents

1.	General description	1
2.	Features and benefits	. 1
3.	Applications	. 1
4.	Pinning information	2
5.	Ordering information	2
6.	Marking	2
7.	Limiting values	. 3
8.	Characteristics	3
9.	Application information	. 6
10.	Package outline	. 6
11.	Soldering	. 6
12.	Revision history	8
	Legal information	

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