

# FDMS007N08LC

## N-Channel Shielded Gate POWER trench<sup>®</sup> MOSFET

80 V, 84 A, 6.7 mΩ

### Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced POWER trench process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 6.7 mΩ at  $V_{GS} = 10$  V,  $I_D = 21$  A
- Max  $r_{DS(on)}$  = 9.9 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 17$  A
- 50% Lower  $Q_{rr}$  than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

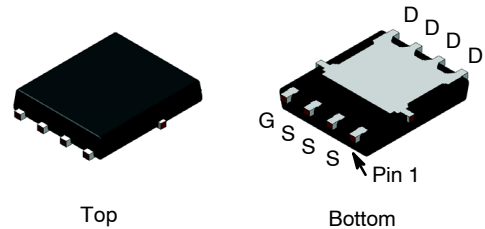
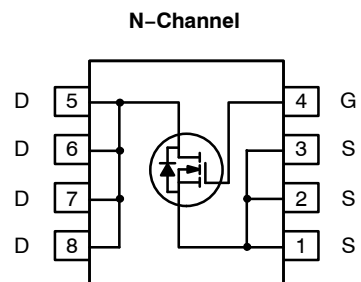
- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar



ON Semiconductor<sup>®</sup>

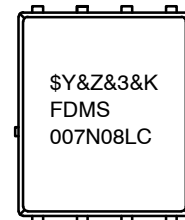
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$V_{DS}$	$r_{DS(on)}$ MAX	$I_D$ MAX
80 V	6.7 mΩ @ 10 V	84 A



PQFN8 5x6, 1.27P  
(Power 56)  
CASE 483AE

### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
&Z = Assembly Plant Code  
&3 = Numeric Date Code  
&K = Lot Code  
FDMS007N08LC = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDMS007N08LC

## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , Unless otherwise specified)

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage	80	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous $T_C = 25^\circ\text{C}$ (Note 5)	84	A
	– Continuous $T_C = 100^\circ\text{C}$ (Note 5)	53	
	– Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	14	
	– Pulsed (Note 4)	345	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	181.5	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	92.6	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.35	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

## PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping (Qty / Packing) <sup>†</sup>
FDMS007N08LC	FDMS007N08LC	PQFN8 5x6 (Power 56) (Pb-Free/Halogen Free)	13"	12 mm	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , referenced to $25^\circ\text{C}$	–	32	–	mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 64 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	$\pm 100$	$\mu\text{A}$

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 120 \mu\text{A}$	1.0	1.4	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 120 \mu\text{A}$ , referenced to $25^\circ\text{C}$	–	-5.6	–	mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 21 \text{ A}$	–	4.9	6.7	m $\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 17 \text{ A}$	–	6.7	9.9	
		$V_{GS} = 10 \text{ V}, I_D = 21 \text{ A}, T_J = 125^\circ\text{C}$	–	8.5	11.6	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5 \text{ V}, I_D = 21 \text{ A}$	–	84	–	S

# FDMS007N08LC

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	2227	3100	pF
C <sub>oss</sub>	Output Capacitance		–	520	760	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	27	40	pF
R <sub>G</sub>	Gate Resistance		0.1	0.4	0.8	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 21 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	10	21	ns
t <sub>r</sub>	Rise Time		–	3	10	
t <sub>d(off)</sub>	Turn-off Delay Time		–	38	61	
t <sub>f</sub>	Fall Time		–	8	16	
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0V to 10 V, V <sub>DD</sub> = 40 V, I <sub>D</sub> = 21 A	–	33	46	nC
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0V to 4.5 V, V <sub>DD</sub> = 40 V, I <sub>D</sub> = 21 A	–	16	22	nC
Q <sub>gs</sub>	Gate to Source Charge	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 21 A	–	5	–	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	V <sub>DD</sub> = 40 V, I <sub>D</sub> = 21 A	–	4	–	nC
Q <sub>oss</sub>	Output Charge	V <sub>DD</sub> = 40 V, V <sub>GS</sub> = 0 V	–	30	–	nC
Q <sub>sync</sub>	Total Gate Charge Sync	V <sub>DS</sub> = 0 V, I <sub>D</sub> = 21 A	–	35	–	nC

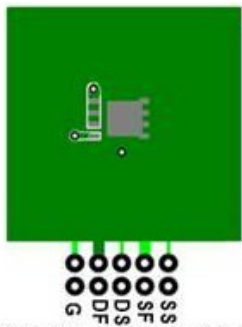
### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.1 A (Note 2)	–	0.7	1.2	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 21 A (Note 2)	–	0.8	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 10 A, di/dt = 300 A/μs	–	18	32	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	24	28	nC
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 10 A, di/dt = 1000 A/μs	–	13	23	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	58	92	nC

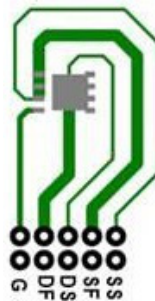
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. R<sub>θCA</sub> is determined by the user's board design.



- a) 50°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



- b) 125°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- E<sub>AS</sub> of 181 mJ is based on starting T<sub>J</sub> = 25°C; L = 3 mH, I<sub>AS</sub> = 11 A, V<sub>DD</sub> = 80 V, V<sub>GS</sub> = 10 V. 100% tested at L = 0.1 mH, I<sub>AS</sub> = 35 A.
- Pulsed I<sub>D</sub> please refer to Fig. 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

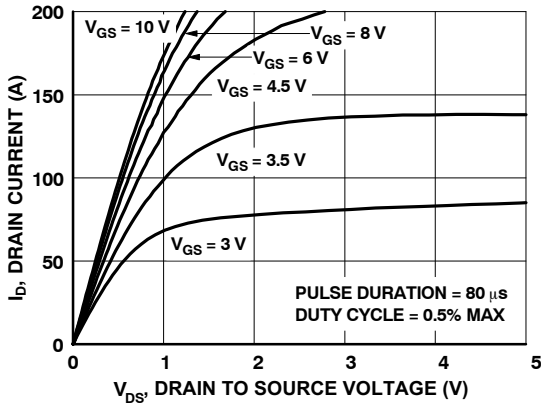


Figure 1. On Region Characteristics

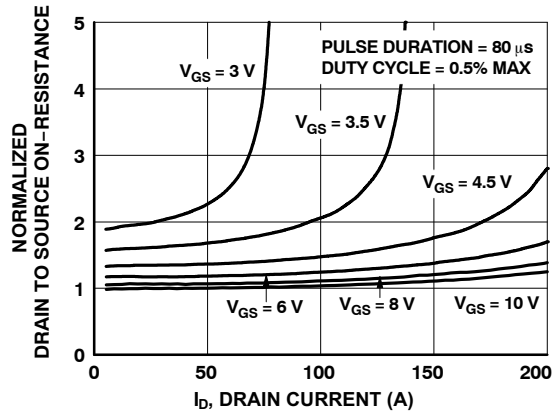


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

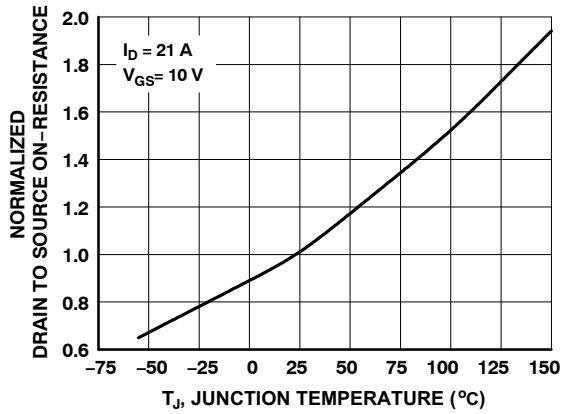


Figure 3. Normalized On Resistance vs. Junction Temperature

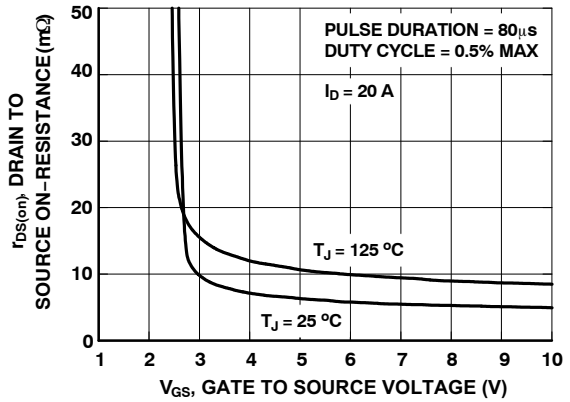


Figure 4. On-Resistance vs. Gate to Source Voltage

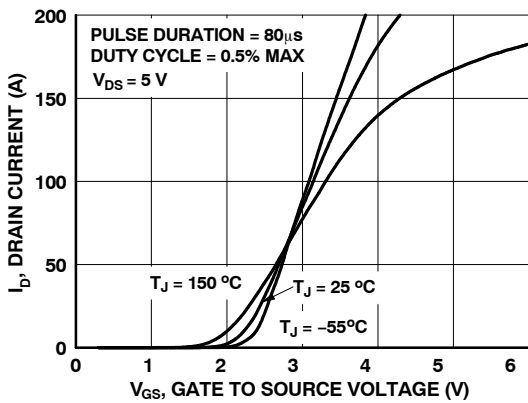


Figure 5. Transfer Characteristics

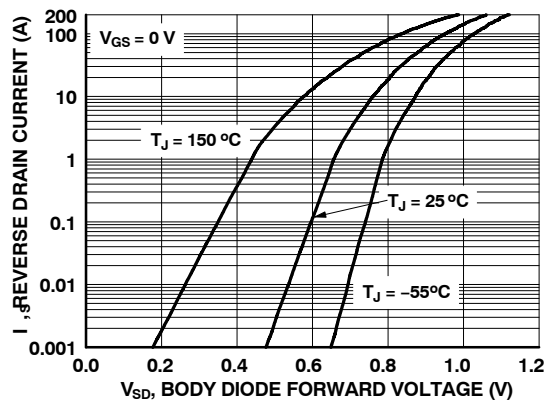


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

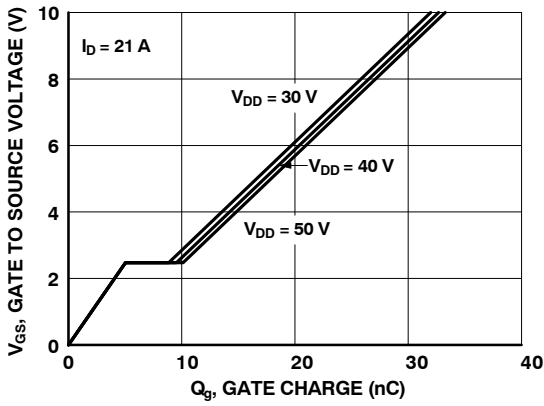


Figure 7. Gate Charge Characteristics

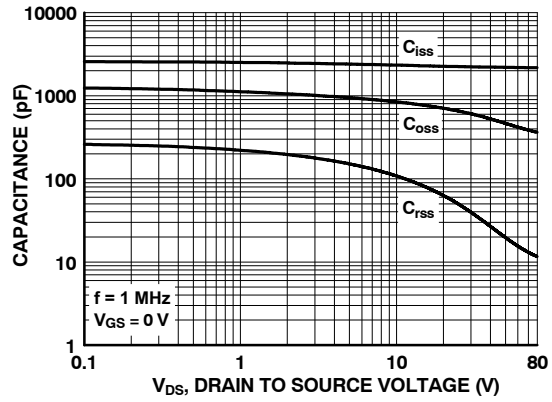


Figure 8. Capacitance vs. Drain to Source Voltage

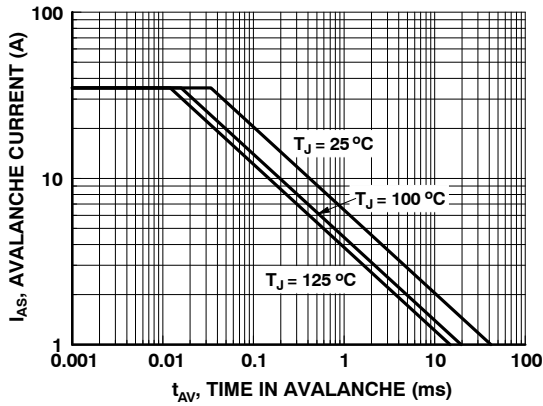


Figure 9. Unclamped Inductive Switching Capability

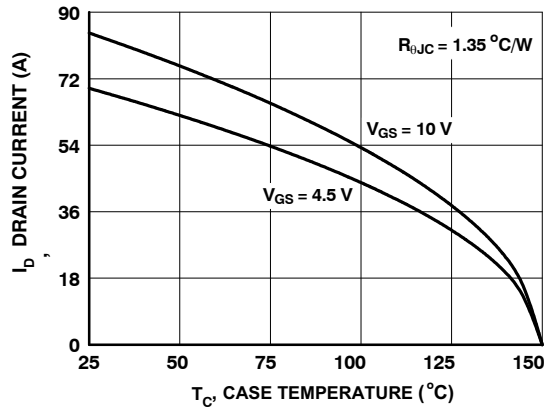


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

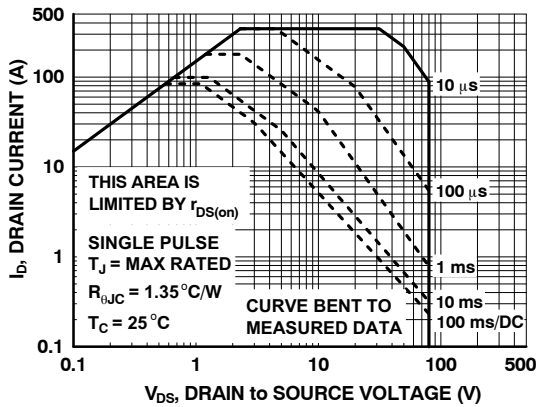


Figure 11. Forward Bias Safe Operating Area

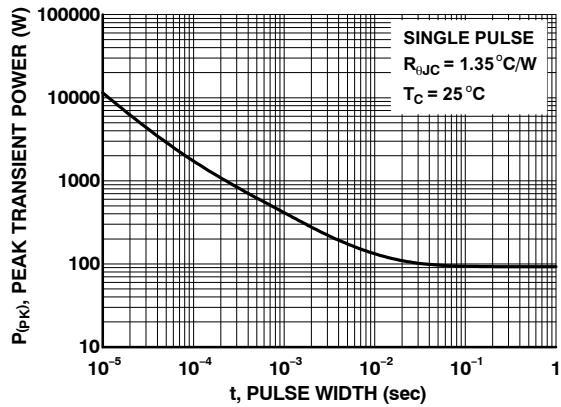


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

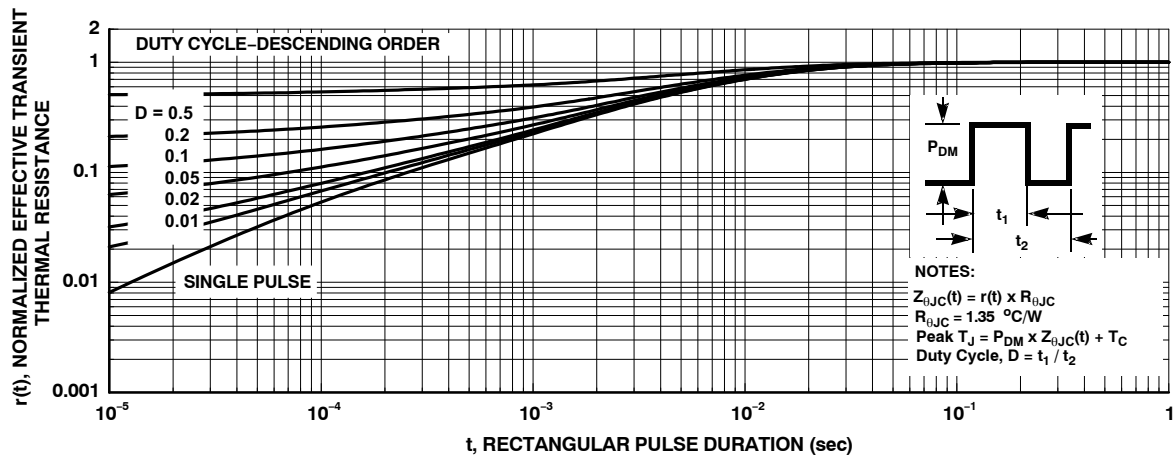
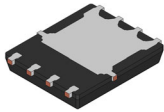


Figure 13. Junction-to-Case Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE

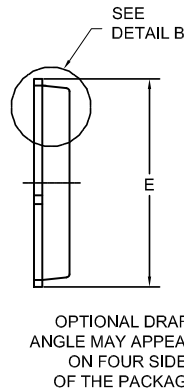
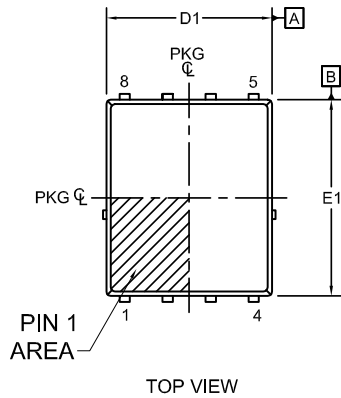
## PACKAGE DIMENSIONS

ON Semiconductor®



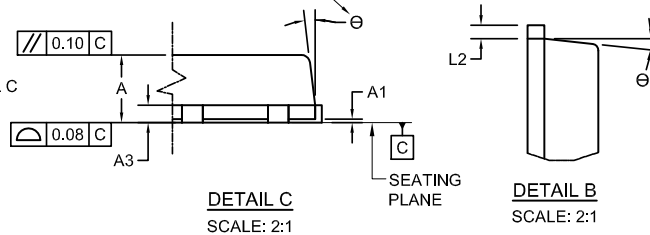
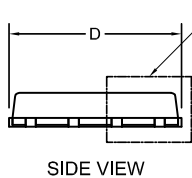
### PQFN8 5X6, 1.27P CASE 483AE ISSUE B

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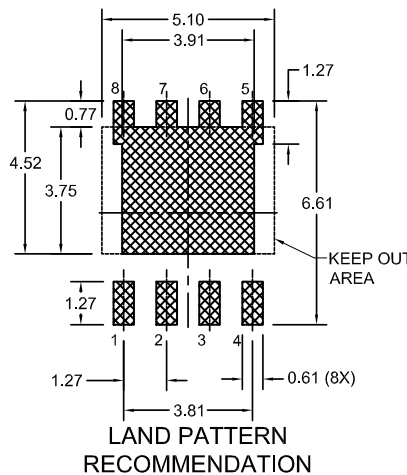
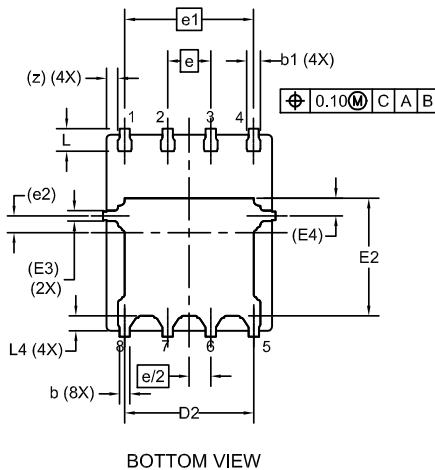


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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