

# 4-Mbit (128 K × 32) Flow-Through Sync SRAM

## Features

- 128 K × 32 common I/O
- 3.3 V core power supply ( $V_{DD}$ )
- 2.5 V or 3.3 V I/O supply ( $V_{DDQ}$ )
- Fast clock-to-output times
  - 8.0 ns (100-MHz version)
- Provide high-performance 2-1-1-1 access rate
- User-selectable burst counter supporting Intel® Pentium® interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- Offered in Pb-free 100-pin TQFP package
- “ZZ” sleep mode option

## Functional Description

The CY7C1338G is a 128 K × 32 synchronous cache RAM designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is

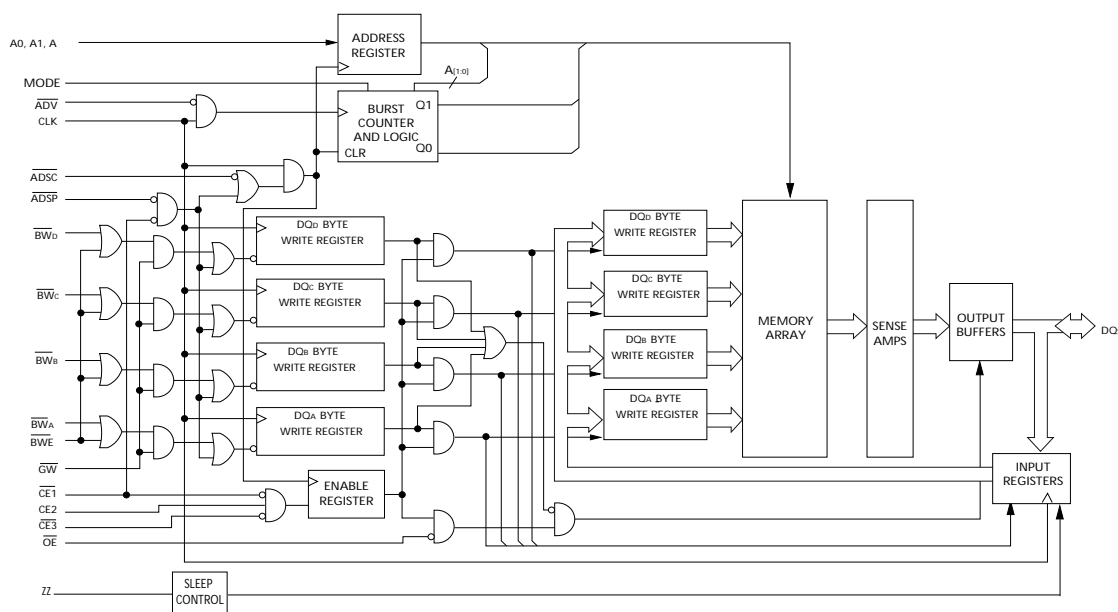
8.0 ns (100-MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable ( $CE_1$ ), depth-expansion chip enables ( $CE_2$  and  $CE_3$ ), burst control inputs (ADSC, ADSP, and ADV), write enables ( $BW_{[A:D]}$  and BWE), and global write (GW). Asynchronous inputs include the output enable (OE) and the ZZ pin.

The CY7C1338G allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the processor address strobe (ADSP) or the cache controller address strobe (ADSC) inputs. Address advancement is controlled by the address advancement (ADV) input.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor (ADSP) or address strobe controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin (ADV).

The CY7C1338G operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

## Logic Block Diagram



**Errata:** For information on silicon errata, see "Errata" on page 19. Details include trigger conditions, devices affected, and proposed workaround.

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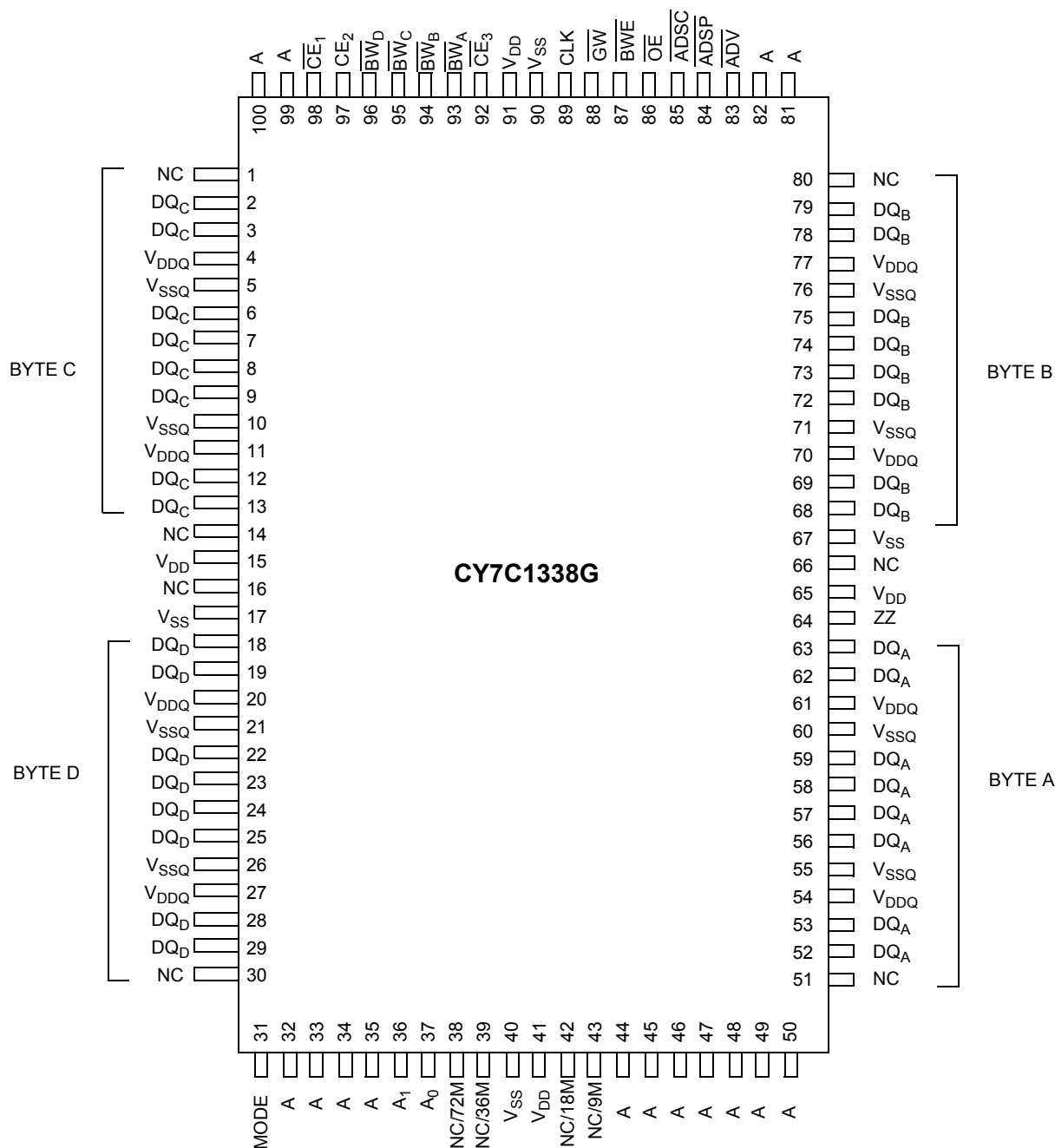
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## Selection Guide

Description	100 MHz	Unit
Maximum access time	8.0	ns
Maximum operating current	205	mA
Maximum standby current	40	mA

## Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout<sup>[1]</sup>



### Note

- Errata:** The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see "Errata" on page 19.

## Pin Definitions

Name	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input-synchronous	<b>Address inputs used to select one of the 128 K address locations.</b> Sampled at the rising edge of the CLK if ADSP or ADSC is active LOW, and CE <sub>1</sub> , CE <sub>2</sub> , and CE <sub>3</sub> are sampled active. A <sub>[1:0]</sub> feed the 2-bit counter.
$\overline{BW}_A$ , $\overline{BW}_B$ , $\overline{BW}_C$ , $\overline{BW}_D$	Input-synchronous	<b>Byte write select inputs, active LOW.</b> Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-synchronous	<b>Global write enable input, active LOW.</b> When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$ ).
$\overline{BWE}$	Input-synchronous	<b>Byte write enable input, active LOW.</b> Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-clock	<b>Clock input.</b> Used to capture all synchronous inputs to the device. Also used to increment the burst counter when ADV is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input-synchronous	<b>Chip enable 1 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with CE <sub>2</sub> and CE <sub>3</sub> to select/deselect the device. ADSP is ignored if CE <sub>1</sub> is HIGH. CE <sub>1</sub> is sampled only when a new external address is loaded.
CE <sub>2</sub>	Input-synchronous	<b>Chip enable 2 input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE <sub>3</sub> to select/deselect the device. CE <sub>2</sub> is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input-synchronous	<b>Chip enable 3 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE <sub>2</sub> to select/deselect the device. CE <sub>3</sub> is sampled only when a new external address is loaded.
$\overline{OE}$	Input-asynchronous	<b>Output enable, asynchronous input, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. OE is masked during the first clock of a read cycle when emerging from a deselected state.
ADV	Input-synchronous	<b>Advance input signal, sampled on the rising edge of CLK.</b> When asserted, it automatically increments the address in a burst cycle.
ADSP	Input-synchronous	<b>Address strobe from processor, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized. ADSP is ignored when CE <sub>1</sub> is deasserted HIGH.
ADSC	Input-synchronous	<b>Address strobe from controller, sampled on the rising edge of CLK, active LOW.</b> When asserted LOW, addresses presented to the device are captured in the address registers. A <sub>[1:0]</sub> are also loaded into the burst counter. When ADSP and ADSC are both asserted, only ADSP is recognized.
ZZ <sup>[2]</sup>	Input-asynchronous	<b>ZZ “sleep” input, active HIGH.</b> When asserted HIGH places the device in a non-time-critical “sleep” condition with data integrity preserved. During normal operation, this pin has to be low or left floating. ZZ pin has an internal pull-down.
DQs	I/O-synchronous	<b>Bidirectional data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by OE. When OE is asserted LOW, the pins behave as outputs. When HIGH, DQs are placed in a tri-state condition.
V <sub>DD</sub>	Power supply	<b>Power supply inputs to the core of the device.</b>
V <sub>SS</sub>	Ground	<b>Ground for the core of the device.</b>
V <sub>DDQ</sub>	I/O power supply	<b>Power supply for the I/O circuitry.</b>
V <sub>SSQ</sub>	I/O ground	<b>Ground for the I/O circuitry.</b>
MODE	Input-static	<b>Selects burst order.</b> When tied to GND selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up.

### Note

2. **Errata:** The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see “Errata” on page 19.

## Pin Definitions *(continued)*

Name	I/O	Description
NC		<b>No connects.</b> Not Internally connected to the die.
NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, NC/1G	–	<b>No connects.</b> Not internally connected to the die. NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M and NC/1G are address expansion pins that are not internally connected to the die.

## Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise ( $t_{CO}$ ) is 8.0 ns (100-MHz device).

The CY7C1338G supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486™ processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe (ADSP) or the controller address strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable (BWE) and byte write select ( $BW_{[A:D]}$ ) inputs. A global write enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ( $\overline{CE}_1$ ,  $CE_2$ ,  $\overline{CE}_3$ ) and an asynchronous output enable ( $\overline{OE}$ ) provide for easy bank selection and output tri-state control. ADSP is ignored if  $\overline{CE}_1$  is HIGH.

### Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ ,  $CE_2$ , and  $CE_3$  are all asserted active, and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the  $\overline{OE}$  input is asserted LOW, the requested data will be available at the data outputs a maximum of  $t_{CDV}$  after clock rise. ADSP is ignored if  $\overline{CE}_1$  is HIGH.

### Single Write Accesses Initiated by ADSP

This access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ ,  $CE_2$ ,  $CE_3$  are all asserted active, and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, BWE, and  $BW_{[A:D]}$ ) are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the

appropriate data will be latched and written into the device. Byte writes are allowed. During byte writes,  $BW_A$  controls  $DQ_A$  and  $BW_B$  controls  $DQ_B$ .  $BW_C$  controls  $DQ_C$ , and  $BW_D$  controls  $DQ_D$ . All I/Os are tri-stated during a byte write. Since this is a common I/O device, the asynchronous  $\overline{OE}$  input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Single Write Accesses Initiated by ADSC

This write access is initiated when the following conditions are satisfied at clock rise: (1)  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{CE}_3$  are all asserted active, (2) ADSC is asserted LOW, (3) ADSP is deasserted HIGH, and (4) the write input signals (GW, BWE, and  $BW_{[A:D]}$ ) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to  $DQ_{[A:D]}$  will be written into the specified address location. Byte writes are allowed. During byte writes,  $BW_A$  controls  $DQ_A$ ,  $BW_B$  controls  $DQ_B$ ,  $BW_C$  controls  $DQ_C$ , and  $BW_D$  controls  $DQ_D$ . All I/Os are tri-stated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous  $\overline{OE}$  input signal must be deasserted and the I/Os must be tri-stated prior to the presentation of data to DQs. As a safety precaution, the data lines are tri-stated once a write cycle is detected, regardless of the state of  $\overline{OE}$ .

### Burst Sequences

The CY7C1338G provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by  $A[1:0]$ , and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE will select a linear burst sequence. A HIGH on MODE will select an interleaved burst order. Leaving MODE unconnected will cause the device to default to a interleaved burst sequence.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode.  $\overline{CE}$ s, ADSP, and ADSC must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

**Interleaved Burst Address Table**

 (MODE = Floating or  $V_{DD}$ )

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

**Linear Burst Address Table**

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

**ZZ Mode Electrical Characteristics**

Parameter	Description	Test Conditions	Min	Max	Unit
$I_{DDZZ}$	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2 \text{ V}$	–	40	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2 \text{ V}$	–	$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2 \text{ V}$	$2t_{CYC}$	–	ns
$t_{ZZI}$	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
$t_{RZZI}$	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns

## Truth Table

The truth table for CY7C1338G follows. [3, 4, 5, 6, 7]

Cycle Description	Address Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	X	X	L	X	L	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	L	X	L	L	X	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	X	H	L	L	X	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	L	L	X	L	H	L	X	X	X	L-H	Tri-state
Deselected cycle, power-down	None	X	X	X	L	H	L	X	X	X	L-H	Tri-state
Sleep mode, power-down	None	X	X	X	H	X	X	X	X	X	X	Tri-state
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	L	X	X	X	H	L-H	Tri-state
Write cycle, begin burst	External	L	H	L	L	H	L	X	L	X	L-H	D
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	L	L-H	Q
Read cycle, begin burst	External	L	H	L	L	H	L	X	H	H	L-H	Tri-state
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	X	X	X	L	H	H	L	H	H	L-H	Tri-state
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
Read cycle, continue burst	Next	H	X	X	L	X	H	L	H	H	L-H	Tri-state
Write cycle, continue burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
Write cycle, continue burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	X	X	X	L	H	H	H	H	H	L-H	Tri-state
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
Read cycle, suspend burst	Current	H	X	X	L	X	H	H	H	H	L-H	Tri-state
Write cycle, suspend burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
Write cycle, suspend burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

### Notes

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.
- $\overline{WRITE} = L$  when any one or more byte write enable signals ( $\overline{BW}_A$ ,  $\overline{BW}_B$ ,  $\overline{BW}_C$ ,  $\overline{BW}_D$ ) and  $\overline{BWE} = L$  or  $\overline{GW} = L$ .  $\overline{WRITE} = H$  when all byte write enable signals ( $\overline{BW}_A$ ,  $\overline{BW}_B$ ,  $\overline{BW}_C$ ,  $\overline{BW}_D$ ),  $\overline{BWE}$ ,  $\overline{GW} = H$ .
- The DQ pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
- The SRAM always initiates a read cycle when  $\overline{ADSP}$  is asserted, regardless of the state of  $\overline{GW}$ ,  $\overline{BWE}$ , or  $\overline{BW}_X$ . Writes may occur only on subsequent clocks after the  $\overline{ADSP}$  or with the assertion of  $\overline{ADSC}$ . As a result,  $\overline{OE}$  must be driven HIGH prior to the start of the write cycle to allow the outputs to tri-state.  $\overline{OE}$  is a don't care for the remainder of the write cycle.
- $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tri-state when  $\overline{OE}$  is inactive or when the device is deselected, and all data bits behave as output when  $\overline{OE}$  is active (LOW).

## Partial Truth Table for Read/Write

The partial truth table for Read/Write for CY7C1338G follows. [8, 9]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write byte A	H	L	H	H	H	L
Write byte B	H	L	H	H	L	H
Write bytes B, A	H	L	H	H	L	L
Write byte C	H	L	H	L	H	H
Write bytes C, A	H	L	H	L	H	L
Write bytes C, B	H	L	H	L	L	H
Write bytes C, B, A	H	L	H	L	L	L
Write byte D	H	L	L	H	H	H
Write bytes D, A	H	L	L	H	H	L
Write bytes D, B	H	L	L	H	L	H
Write bytes D, B, A	H	L	L	H	L	L
Write bytes D, B	H	L	L	L	H	H
Write bytes D, B, A	H	L	L	L	H	L
Write bytes D, C, A	H	L	L	L	L	H
Write all bytes	H	L	L	L	L	L
Write all bytes	L	X	X	X	X	X

### Notes

8. X = "Don't Care." H = Logic HIGH, L = Logic LOW.

9. Table only lists a partial listing of the byte write combinations. Any combination of  $\overline{BW_x}$  is valid. Appropriate write will be done based on which byte write is active.



## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{DD}$  relative to GND ..... -0.5 V to +4.6 V

Supply voltage on  $V_{DDQ}$  relative to GND ..... -0.5 V to + $V_{DD}$

DC voltage applied to outputs in tri-state ..... -0.5 V to  $V_{DDQ} + 0.5$  V

DC input voltage ..... -0.5 V to  $V_{DD} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{DD}$	$V_{DDQ}$
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to $V_{DD}$

## Electrical Characteristics

Over the Operating Range

Parameter <sup>[10, 11]</sup>	Description	Test Conditions	Min	Max	Unit
$V_{DD}$	Power supply voltage		3.135	3.6	V
$V_{DDQ}$	I/O supply voltage		2.375	$V_{DD}$	V
$V_{OH}$	Output HIGH voltage	for 3.3 V I/O, $I_{OH} = -4.0$ mA for 2.5 V I/O, $I_{OH} = -1.0$ mA	2.4 2.0	–	V
$V_{OL}$	Output LOW voltage	for 3.3 V I/O, $I_{OL} = 8.0$ mA for 2.5 V I/O, $I_{OL} = 1.0$ mA	– –	0.4 0.4	V
$V_{IH}$	Input HIGH voltage	for 3.3 V I/O for 2.5 V I/O	2.0 1.7	$V_{DD} + 0.3$ $V_{DD} + 0.3$	V
$V_{IL}$	Input LOW voltage <sup>[10]</sup>	for 3.3 V I/O for 2.5 V I/O	–0.3 –0.3	0.8 0.7	V
$I_X$	Input leakage current except ZZ and MODE	$GND \leq V_I \leq V_{DDQ}$	–5	5	μA
	Input current of MODE	Input = $V_{SS}$	–30	–	μA
		Input = $V_{DD}$	–	5	μA
	Input current of ZZ	Input = $V_{SS}$	–5	–	μA
		Input = $V_{DD}$	–	30	μA
$I_{OZ}$	Output leakage current	$GND \leq V_I \leq V_{DDQ}$ , output disabled	–5	5	μA
$I_{DD}$	$V_{DD}$ operating supply current	$V_{DD} = \text{Max}$ , $I_{OUT} = 0$ mA, $f = f_{MAX} = 1/t_{CYC}$	–	205	mA
$I_{SB1}$	Automatic CE power-down current – TTL inputs	Max $V_{DD}$ , device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$ , inputs switching	–	80	mA
$I_{SB2}$	Automatic CE power-down current – CMOS inputs	Max $V_{DD}$ , device deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$ , inputs static	–	40	mA
$I_{SB3}$	Automatic CE power-down current – CMOS inputs	Max $V_{DD}$ , device deselected, $V_{IN} \geq V_{DDQ} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = f_{MAX}$ , inputs switching	–	65	mA
$I_{SB4}$	Automatic CE power-down current – TTL inputs	Max $V_{DD}$ , device deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$ , inputs static	–	45	mA

### Notes

10. Overshoot:  $V_{IH(AC)} < V_{DD} + 1.5$  V (pulse width less than  $t_{CYC}/2$ ), undershoot:  $V_{IL(AC)} > -2$  V (Pulse width less than  $t_{CYC}/2$ ).

11.  $T_{Power-up}$ : Assumes a linear ramp from 0 V to  $V_{DD(min)}$  within 200 ms. During this time  $V_{IH} < V_{DD}$  and  $V_{DDQ} \leq V_{DD}$ .

## Capacitance

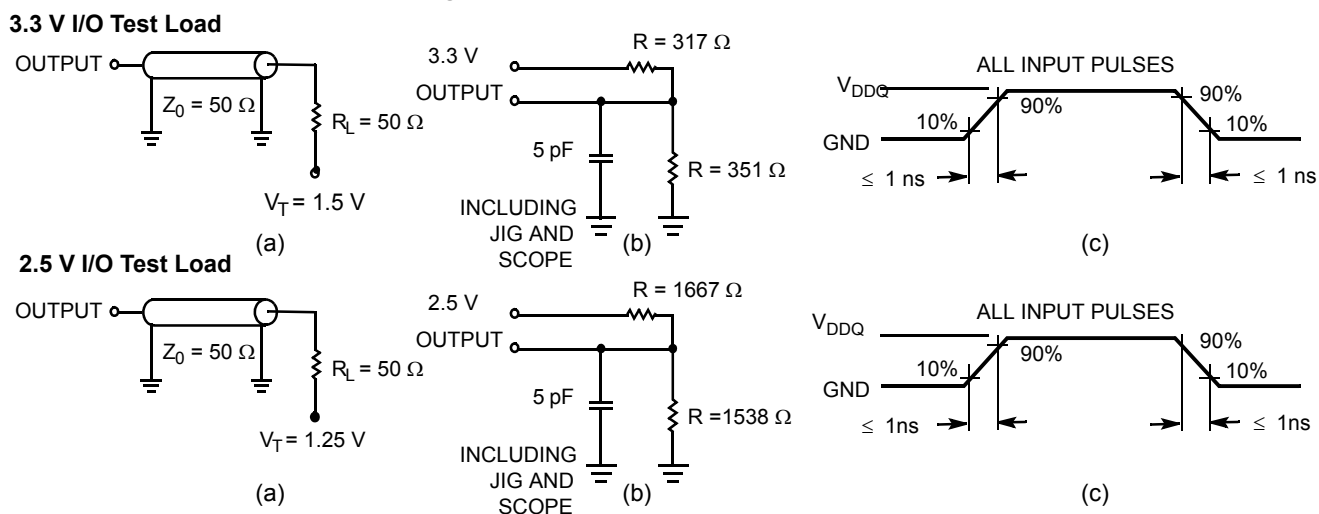
Parameter <sup>[12]</sup>	Description	Test Conditions	100-pin TQFP Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{DD} = 3.3\text{ V}$ , $V_{DDQ} = 3.3\text{ V}$	5	pF
$C_{CLK}$	Clock input capacitance		5	pF
$C_{I/O}$	Input/Output capacitance		5	pF

## Thermal Resistance

Parameter <sup>[12]</sup>	Description	Test Conditions	100-pin TQFP Package	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	30.32	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		6.85	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



### Note

12. Tested initially and after any design or process change that may affect these parameters.

## Switching Characteristics

Over the Operating Range

Parameter <sup>[13, 14]</sup>	Description	-100		Unit
		Min	Max	
t <sub>POWER</sub>	V <sub>DD</sub> (typical) to the first access <sup>[15]</sup>	1	–	ms
<b>Clock</b>				
t <sub>CYC</sub>	Clock cycle time	10	–	ns
t <sub>CH</sub>	Clock HIGH	4.0	–	ns
t <sub>CL</sub>	Clock LOW	4.0	–	ns
<b>Output Times</b>				
t <sub>CDV</sub>	Data output valid after CLK rise	–	8.0	ns
t <sub>DOH</sub>	Data output hold after CLK rise	2.0	–	ns
t <sub>CLZ</sub>	Clock to low Z <sup>[16, 17, 18]</sup>	0	–	ns
t <sub>CHZ</sub>	Clock to high Z <sup>[16, 17, 18]</sup>	–	3.5	ns
t <sub>OE<sub>V</sub></sub>	$\overline{\text{OE}}$ LOW to output valid	–	3.5	ns
t <sub>OE<sub>LZ</sub></sub>	$\overline{\text{OE}}$ LOW to output low Z <sup>[16, 17, 18]</sup>	0	–	ns
t <sub>OE<sub>HZ</sub></sub>	$\overline{\text{OE}}$ HIGH to output high Z <sup>[16, 17, 18]</sup>	–	3.5	ns
<b>Setup Times</b>				
t <sub>AS</sub>	Address set-up before CLK rise	2.0	–	ns
t <sub>ADS</sub>	ADSP, ADSC set-up before CLK rise	2.0	–	ns
t <sub>ADVS</sub>	$\overline{\text{ADV}}$ set-up before CLK rise	2.0	–	ns
t <sub>WES</sub>	$\overline{\text{GW}}$ , BWE, BW <sub>X</sub> set-up before CLK rise	2.0	–	ns
t <sub>DS</sub>	Data input set-up before CLK rise	1.5	–	ns
t <sub>CES</sub>	Chip enable set-up	2.0	–	ns
<b>Hold Times</b>				
t <sub>AH</sub>	Address hold after CLK rise	0.5	–	ns
t <sub>ADH</sub>	$\overline{\text{ADSP}}$ , $\overline{\text{ADSC}}$ hold after CLK rise	0.5	–	ns
t <sub>WEH</sub>	$\overline{\text{GW}}$ , BWE, BW <sub>X</sub> hold after CLK rise	0.5	–	ns
t <sub>ADVH</sub>	$\overline{\text{ADV}}$ hold after CLK rise	0.5	–	ns
t <sub>DH</sub>	Data input hold after CLK rise	0.5	–	ns
t <sub>CEH</sub>	Chip enable hold after CLK rise	0.5	–	ns

### Notes

13. Timing reference level is 1.5 V when V<sub>DDQ</sub> = 3.3 V and is 1.25 V when V<sub>DDQ</sub> = 2.5 V.

14. Test conditions shown in (a) of [Figure 2 on page 10](#) unless otherwise noted.

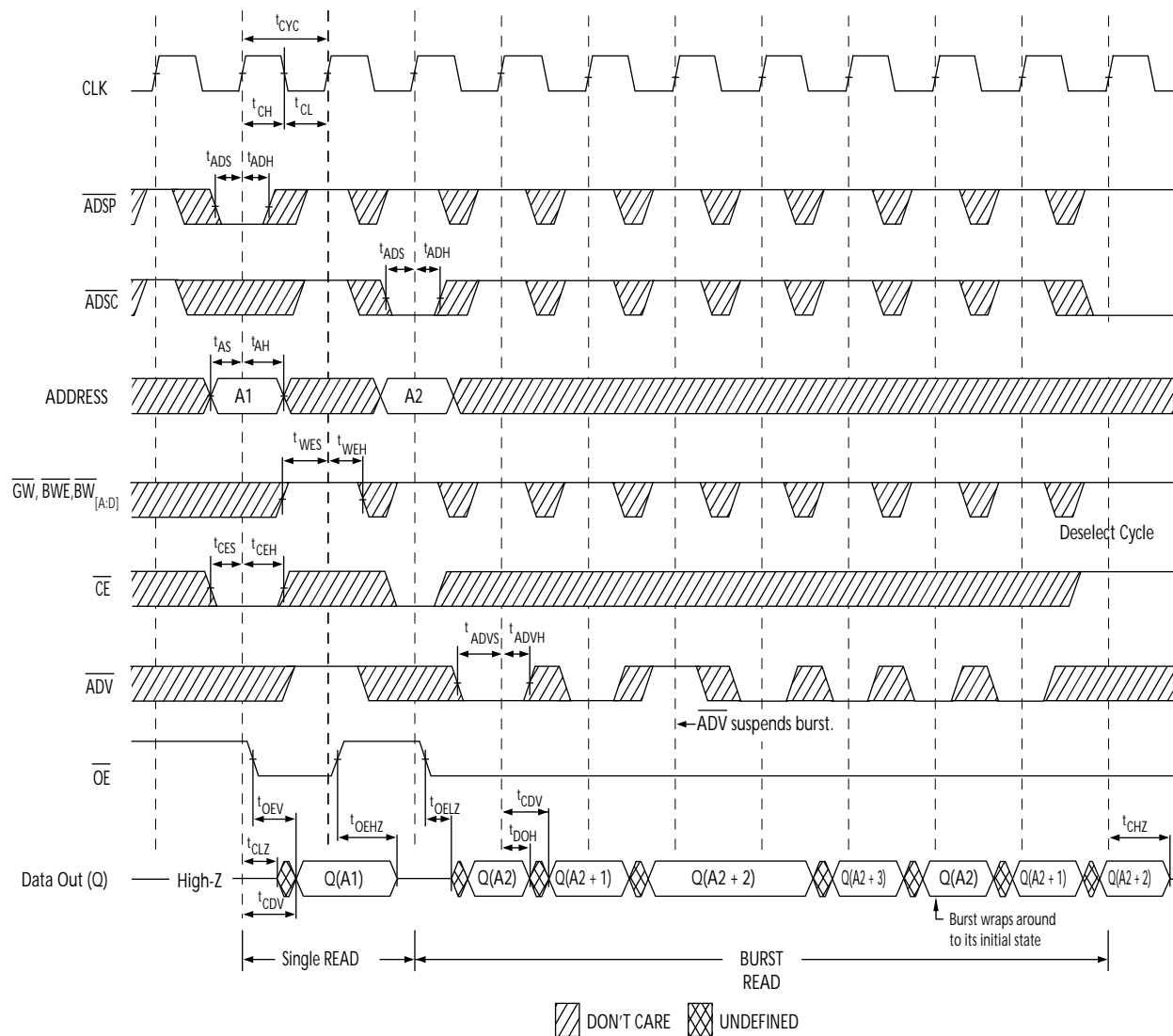
15. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power needs to be supplied above V<sub>DD(minimum)</sub> initially before a read or write operation can be initiated.

16. t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>OE<sub>LZ</sub></sub>, and t<sub>OE<sub>HZ</sub></sub> are specified with AC test conditions shown in part (b) of [Figure 2 on page 10](#). Transition is measured ±200 mV from steady-state voltage.

17. At any given voltage and temperature, t<sub>OE<sub>HZ</sub></sub> is less than t<sub>OE<sub>LZ</sub></sub> and t<sub>CHZ</sub> is less than t<sub>CLZ</sub> to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.

18. This parameter is sampled and not 100% tested.

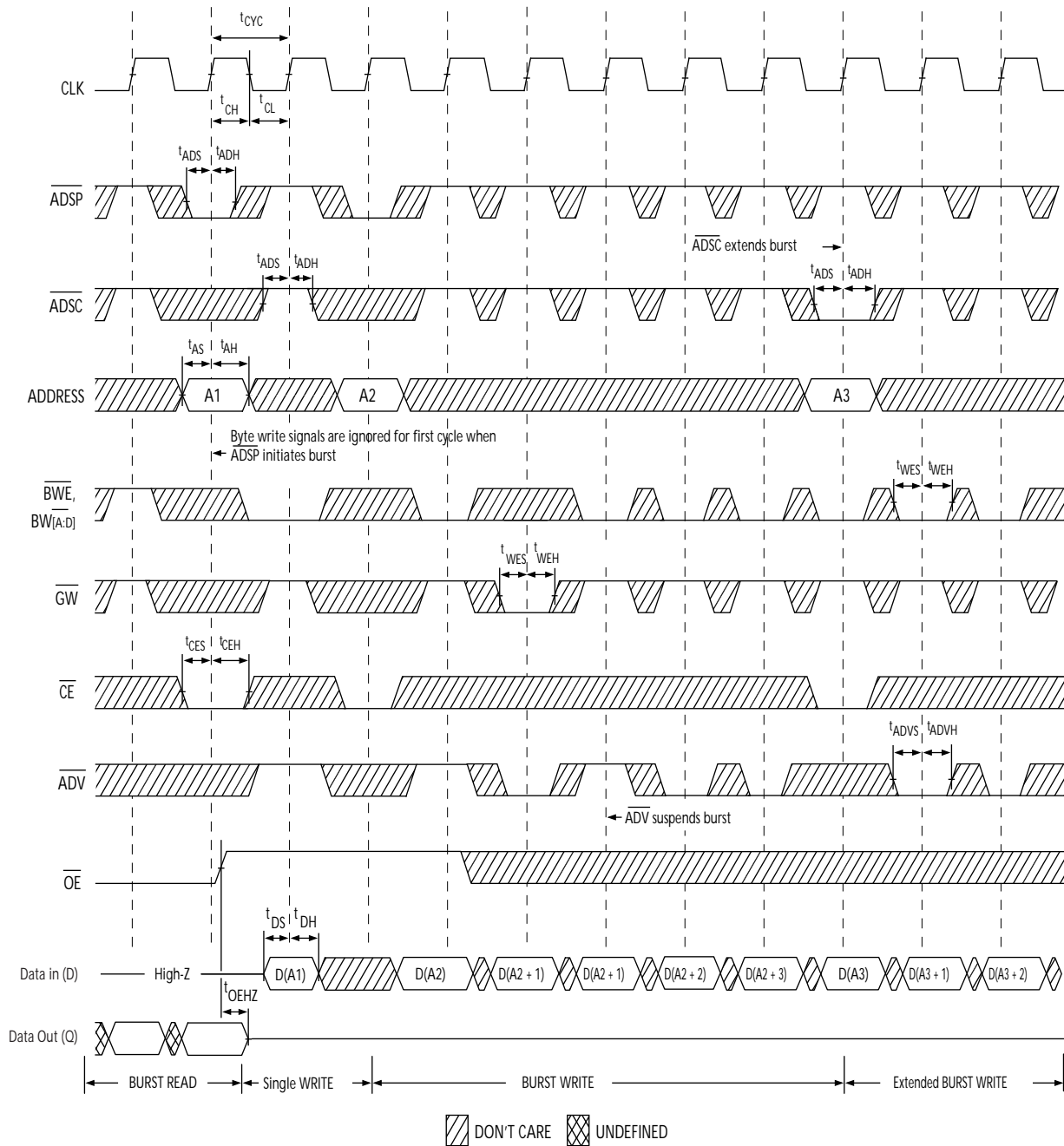
**Figure 3. Read Cycle Timing**<sup>[19]</sup>



**Note**  
19. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.

## Timing Diagrams (continued)

**Figure 4. Write Cycle Timing** [20, 21]



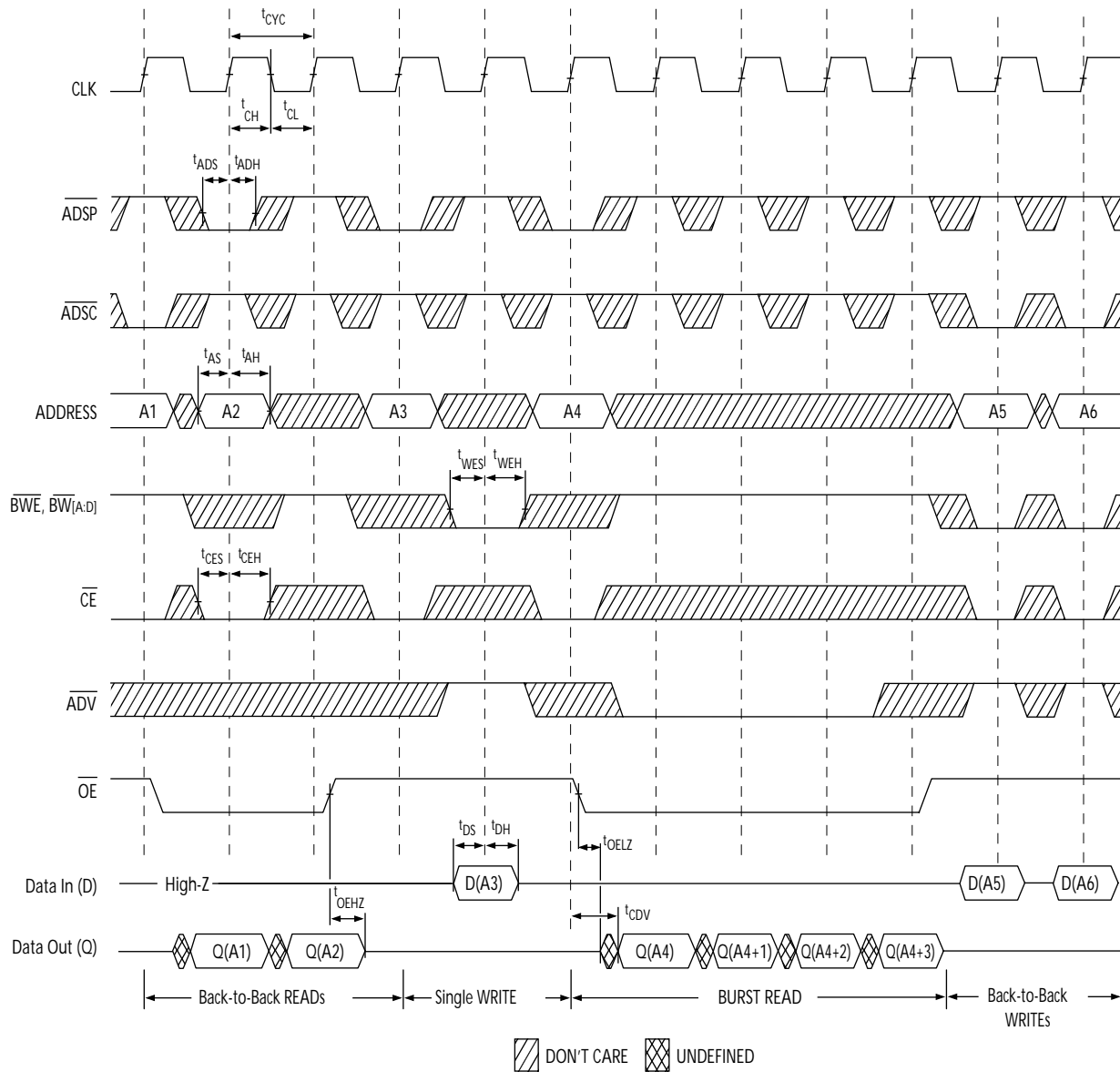
### Notes

20. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW or  $\overline{CE}_3$  is HIGH.

21. Full width write can be initiated by either GW LOW; or by GW HIGH, BWE LOW and  $BW_{[A:D]}$  LOW.

## Timing Diagrams (continued)

**Figure 5. Read/Write Timing** [22, 23, 24]

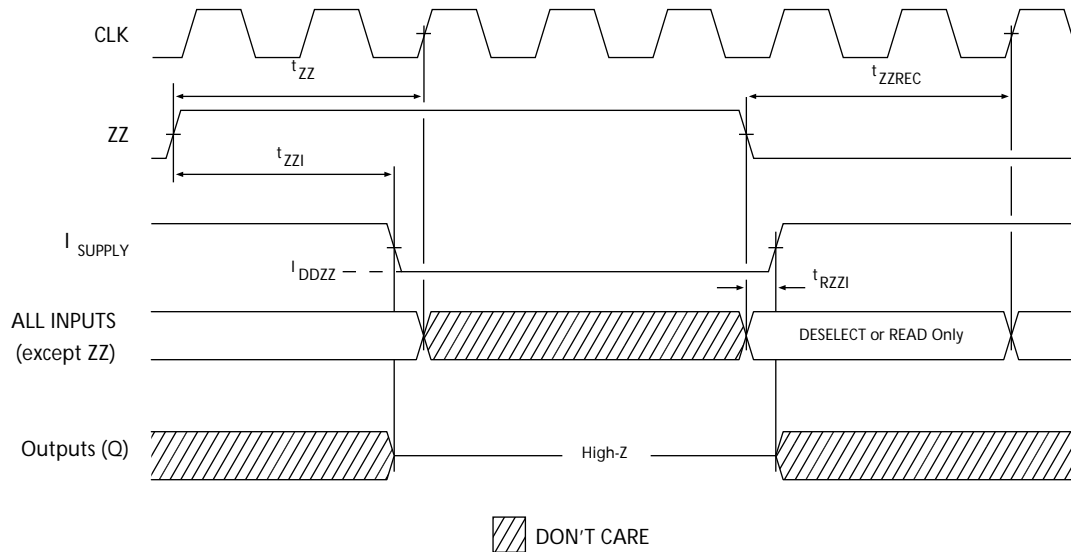


### Notes

22. On this diagram, when  $\overline{CE}$  is LOW:  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH:  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.  
 23. The data bus (Q) remains in high Z following a WRITE cycle, unless a new read access is initiated by ADSP or ADSC.  
 24.  $\overline{GW}$  is HIGH.

## Timing Diagrams *(continued)*

**Figure 6. ZZ Mode Timing** [25, 26]



### Notes

- 25. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
- 26. DQs are in high Z when exiting ZZ sleep mode.

## Ordering Information

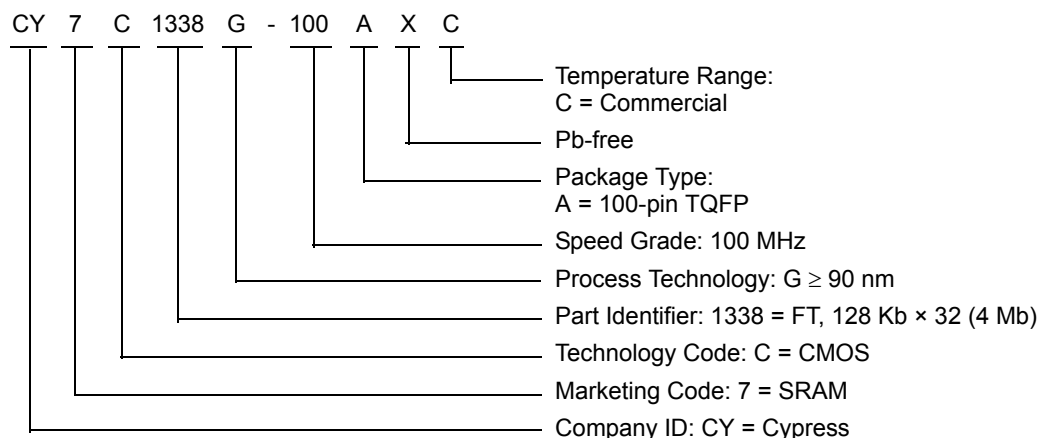
Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.

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Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
100	CY7C1338G-100AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial

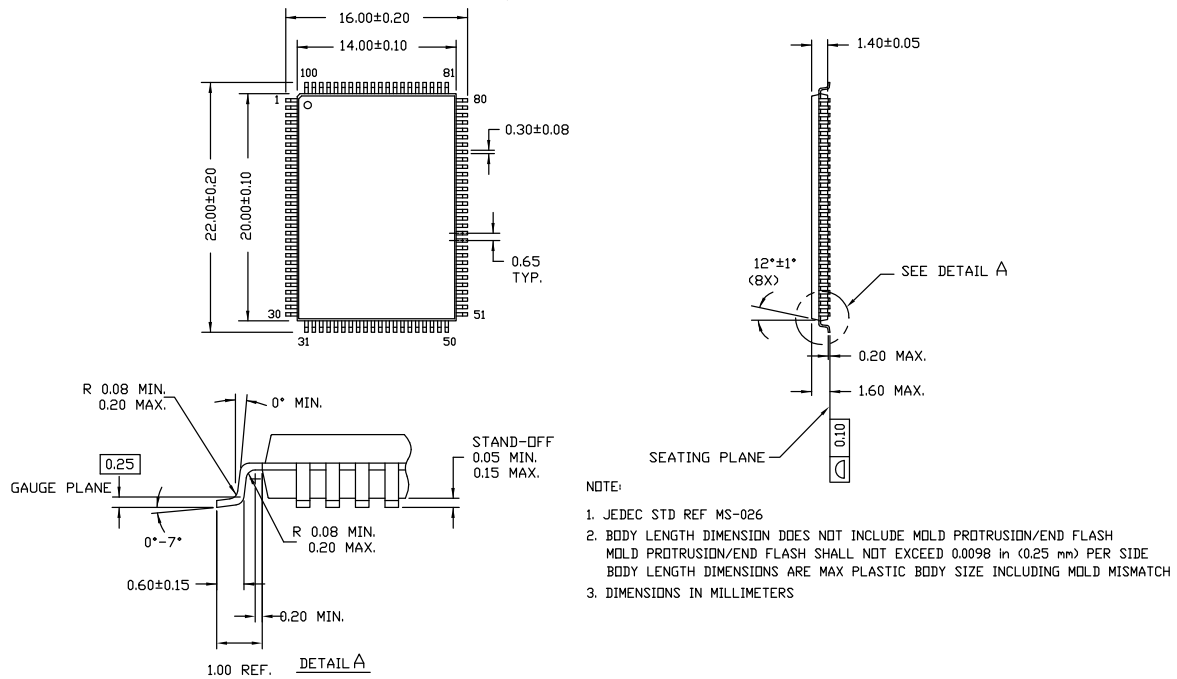
## Ordering Code Definitions





## Package Diagrams

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



51-85050 \*D

## Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius
MHz	megahertz
$\mu\text{A}$	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
nm	nanometer
ns	nanosecond
$\Omega$	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Errata

This section describes the Ram9 Sync/NoBL ZZ pin, JTAG and Chip Enable issues. Details include trigger conditions, the devices affected, proposed workaround and silicon revision applicability. Please contact your local Cypress sales representative if you have further questions.

### Part Numbers Affected

Density & Revision	Package Type	Operating Range
4Mb-Ram9 Synchronous SRAMs: CY7C133*G	All packages	Commercial/ Industrial

### Product Status

All of the devices in the Ram9 4Mb Sync/NoBL family are qualified and available in production quantities.

### Ram9 Sync/NoBL ZZ Pin Issues Errata Summary

The following table defines the errata applicable to available Ram9 4Mb Sync/NoBL family devices.

Item	Issues	Description	Device	Fix Status
1.	ZZ Pin	When asserted HIGH, the ZZ pin places device in a "sleep" condition with data integrity preserved. The ZZ pin currently does not have an internal pull-down resistor and hence cannot be left floating externally by the user during normal mode of operation.	4M-Ram9 (90nm)	For the 4M Ram9 (90 nm) devices, there is no plan to fix this issue.

#### 1. ZZ Pin Issue

##### ■ PROBLEM DEFINITION

The problem occurs only when the device is operated in the normal mode with ZZ pin left floating. The ZZ pin on the SRAM device does not have an internal pull-down resistor. Switching noise in the system may cause the SRAM to recognize a HIGH on the ZZ input, which may cause the SRAM to enter sleep mode. This could result in incorrect or undesirable operation of the SRAM.

##### ■ TRIGGER CONDITIONS

Device operated with ZZ pin left floating.

##### ■ SCOPE OF IMPACT

When the ZZ pin is left floating, the device delivers incorrect data.

##### ■ WORKAROUND

Tie the ZZ pin externally to ground.

##### ■ FIX STATUS

Fix was done for the 72Mb RAM9 Synchronous SRAMs and 72M RAM9 NoBL SRAMs devices. Fixed devices have a new revision. The following table lists the devices affected and the new revision after the fix.

## Document History Page

Document Title: CY7C1338G, 4-Mbit (128 K × 32) Flow-Through Sync SRAM Document Number: 38-05521				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	224369	See ECN	RKF	New data sheet.
*A	278513	See ECN	VBL	Updated <a href="#">Features</a> (Removed 66 MHz frequency related information). Updated <a href="#">Selection Guide</a> (Removed 66 MHz frequency related information). Updated <a href="#">Electrical Characteristics</a> (Removed 66 MHz frequency related information). Updated <a href="#">Switching Characteristics</a> (Removed 66 MHz frequency related information). Updated <a href="#">Ordering Information</a> (Updated part numbers (Added Pb-free BGA package), changed TQFP package to Pb-free TQFP package, added comment on the BGA Pb-free package availability below the table).
*B	333626	See ECN	SYT	Updated <a href="#">Features</a> (Removed 117 MHz frequency related information). Updated <a href="#">Selection Guide</a> (Removed 117 MHz frequency related information). Updated <a href="#">Pin Configurations</a> (Modified Address Expansion balls in the pinouts for 100-pin TQFP and 119-ball BGA Packages as per JEDEC standards). Updated <a href="#">Pin Definitions</a> . Updated <a href="#">Functional Overview</a> (Updated <a href="#">ZZ Mode Electrical Characteristics</a> (Replaced 'Snooze' with 'Sleep')). Updated <a href="#">Truth Table</a> (Replaced 'Snooze' with 'Sleep'). Updated <a href="#">Electrical Characteristics</a> (Updated test conditions for $V_{OL}$ and $V_{OH}$ parameters, removed 117 MHz frequency related information). Updated <a href="#">Thermal Resistance</a> (Replaced TBD's for $\Theta_{JA}$ and $\Theta_{JC}$ to their respective values). Updated <a href="#">Ordering Information</a> (By shading and unshading MPNs as per availability, removed comment on the availability of BGA Pb-free package).
*C	418633	See ECN	R XU	Changed status from Preliminary to Final. Changed address of Cypress Semiconductor Corporation from "3901 North First Street" to "198 Champion Court". Updated <a href="#">Electrical Characteristics</a> (Removed $I_{OS}$ parameter and its details, updated Note 11 (Changed test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ ), changed "Input Load Current except ZZ and MODE" to "Input Leakage Current except ZZ and MODE"). Updated <a href="#">Ordering Information</a> (Updated part numbers, replaced Package Name column with Package Diagram in the Ordering Information table). Updated <a href="#">Package Diagrams</a> .
*D	480368	See ECN	VKN	Updated <a href="#">Maximum Ratings</a> (Added the Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND). Updated <a href="#">Ordering Information</a> (Updated part numbers).
*E	2896584	03/20/2010	NJY	Updated <a href="#">Ordering Information</a> (Removed obsolete part numbers). Updated <a href="#">Package Diagrams</a> .
*F	3036754	09/23/2010	NJY	Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Minor edits and updated in new template.
*G	3365114	09/07/2011	PRIT	Updated <a href="#">Package Diagrams</a> .

**Document History Page** *(continued)*

Document Title: CY7C1338G, 4-Mbit (128 K × 32) Flow-Through Sync SRAM Document Number: 38-05521				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
*H	3589101	05/10/2012	NJY / PRIT	Updated <a href="#">Features</a> (Removed 133 MHz frequency related information, removed 119-ball BGA package related information). Updated <a href="#">Functional Description</a> (Removed the Note “For best-practices recommendations, please refer to the Cypress application note <i>System Design Guidelines</i> on <a href="http://www.cypress.com">www.cypress.com</a> .” and its reference, removed 133 MHz frequency related information). Updated <a href="#">Selection Guide</a> (Removed 133 MHz frequency related information). Updated <a href="#">Pin Configurations</a> (Removed 119-ball BGA package related information). Updated <a href="#">Functional Overview</a> (Removed 133 MHz frequency related information). Updated <a href="#">Operating Range</a> (Removed Industrial Temperature Range). Updated <a href="#">Electrical Characteristics</a> (Removed 133 MHz frequency related information). Updated <a href="#">Capacitance</a> (Removed 119-ball BGA package related information). Updated <a href="#">Thermal Resistance</a> (Removed 119-ball BGA package related information). Updated <a href="#">Switching Characteristics</a> (Removed 133 MHz frequency related information). Updated <a href="#">Package Diagrams</a> (Removed 119-ball BGA package related information).
*I	3751125	09/21/2012	PRIT	No technical updates. Completing sunset review.
*J	3984870	05/02/2013	PRIT	Added <a href="#">Errata</a> .
*K	4039556	06/25/2013	PRIT	Added Errata Footnotes. Updated in new template.

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