

## 30V N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD17571Q2](#)

### FEATURES

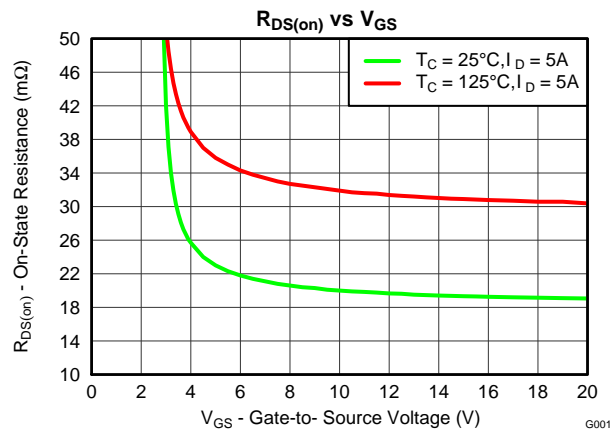
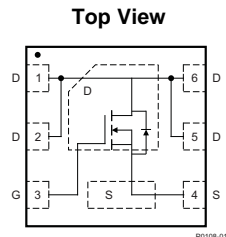
- Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 2-mm × 2-mm Plastic Package

### APPLICATIONS

- Optimized for Load Switch Applications
- Storage, Tablets, and Handheld Devices
- Optimized for Control FET Applications

### DESCRIPTION

This 30V, 20mΩ, Son2x2 NexFET™ power MOSFET has been designed to minimize losses in power conversion and load management applications, while offering excellent thermal performance for the size of the package.



PRODUCT SUMMARY				
$V_{DS}$	Drain to Source Voltage	30		V
$Q_g$	Gate Charge Total (4.5 V)	2.4		nC
$Q_{gd}$	Gate Charge Gate to Drain	0.6		nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}$	24	mΩ
		$V_{GS} = 10\text{ V}$	20	mΩ
$V_{GS(th)}$	Threshold Voltage	1.6		V

### ORDERING INFORMATION

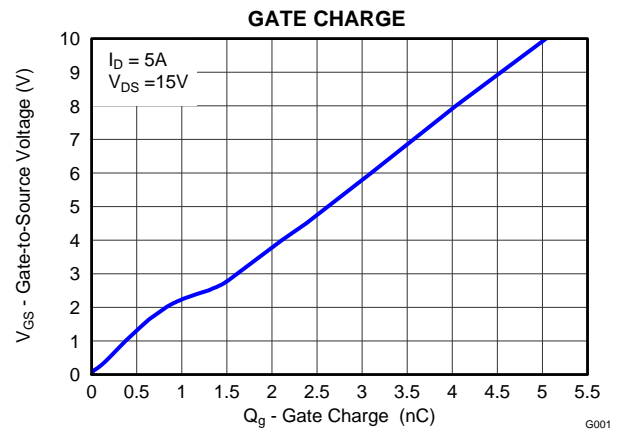
Device	Package	Media	Qty	Ship
CSD17571Q2	SON 2-mm × 2-mm Plastic Package	7-Inch Reel	3000	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Continuous Drain Current (Package Limit)	22	A
	Continuous Drain Current <sup>(1)</sup>	7.6	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	39	A
$P_D$	Power Dissipation <sup>(1)</sup>	2.5	W
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	–55 to 150	°C
$E_{AS}$	Avalanche Energy, single pulse $I_D = 12\text{ A}, L = 0.1\text{ mH}, R_G = 25\text{ }\Omega$	7.2	mJ

(1)  $R_{\theta JA} = 50$  on 1in<sup>2</sup> Cu (2 oz.) on .060" thick FR4 PCB

(2) Pulse duration 10 μs, duty cycle ≤2%



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ , unless otherwise specified

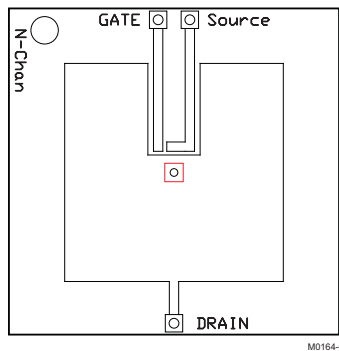
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV <sub>DSS</sub>	Drain to Source Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 24 V	1			μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V	100			nA
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = 250 μA	1.3	1.6	2.0	V
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 4.5 V, I <sub>DS</sub> = 5 A	24		29	mΩ
		V <sub>GS</sub> = 10 V, I <sub>DS</sub> = 5 A	20		24	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 15 V, I <sub>DS</sub> = 5 A	43			S
Dynamic Characteristics						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 15 V, f = 1 MHz	360		468	pF
C <sub>OSS</sub>	Output Capacitance		101		131	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance		9		12	pF
R <sub>g</sub>	Series Gate Resistance		3.8		7.6	Ω
Q <sub>g</sub>	Gate Charge Total (4.5V)	V <sub>DS</sub> = 15 V, I <sub>DS</sub> = 5 A	2.4		3.1	nC
Q <sub>gd</sub>	Gate Charge – Gate to Drain		0.6			nC
Q <sub>gs</sub>	Gate Charge Gate to Source		0.9			nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>		0.6			nC
Q <sub>OSS</sub>	Output Charge	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V	3.4			nC
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>DS</sub> = 5 A R <sub>G</sub> = 2 Ω	5.3			ns
t <sub>r</sub>	Rise Time		19			ns
t <sub>d(off)</sub>	Turn Off Delay Time		8.0			ns
t <sub>f</sub>	Fall Time		2.6			ns
Diode Characteristics						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>DS</sub> = 5 A, V <sub>GS</sub> = 0 V	0.8		1	V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DD</sub> = 15 V, I <sub>F</sub> = 5 A, di/dt = 300 A/μs	2.3			nC
t <sub>rr</sub>	Reverse Recovery Time		11			ns

## THERMAL CHARACTERISTICS

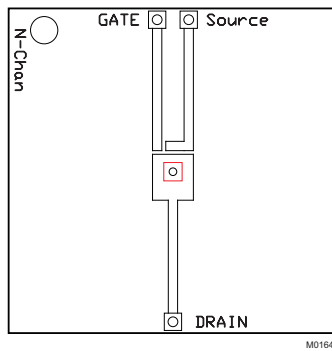
$T_A = 25^\circ\text{C}$  unless otherwise specified

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			6.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			65	$^\circ\text{C}/\text{W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



Max  $R_{\theta JA} = 65$  when  
mounted on 1 inch<sup>2</sup>  
(6.45 cm<sup>2</sup>) of 2-oz.  
(0.071-mm thick) Cu.



Max  $R_{\theta JA} = 235$  when  
mounted on minimum  
pad area of 2-oz.  
(0.071-mm thick) Cu.

## TYPICAL MOSFET CHARACTERISTICS

$T_A = 25^\circ\text{C}$  unless otherwise specified

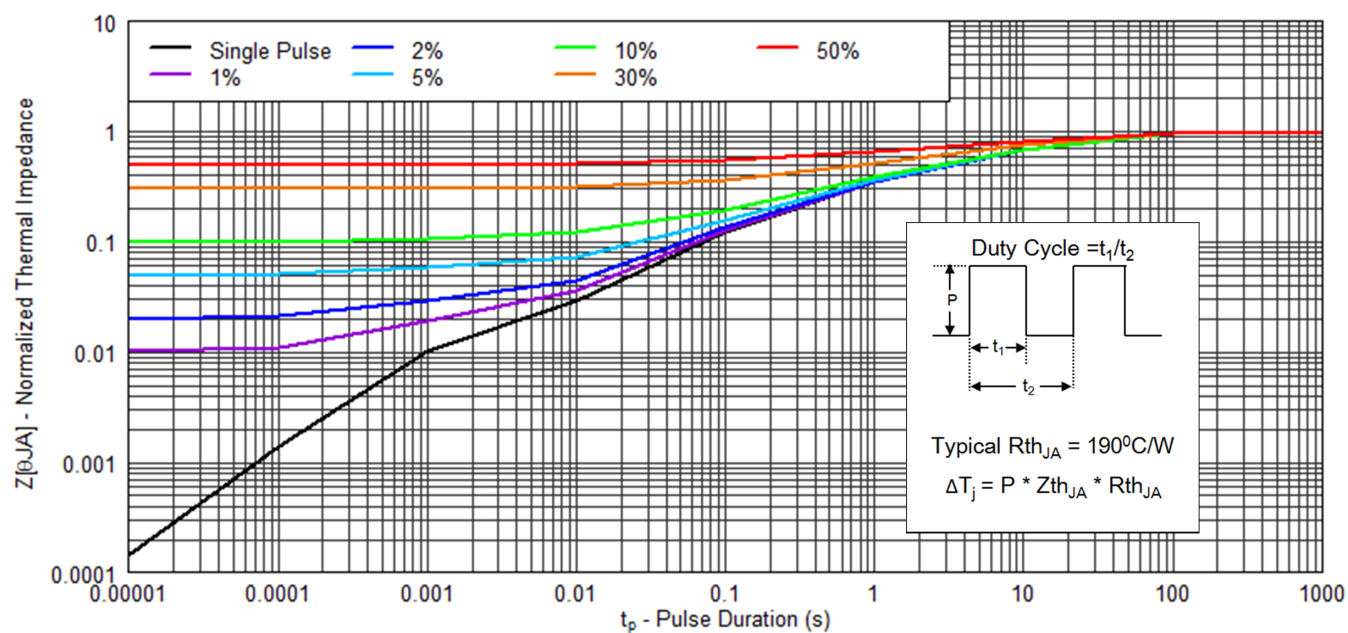


Figure 1. Transient Thermal Impedance

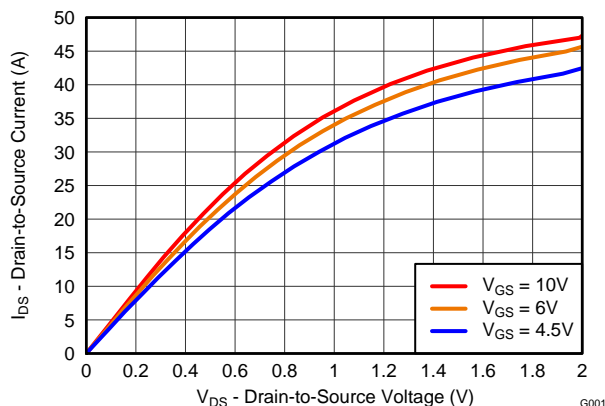


Figure 2. Saturation Characteristics

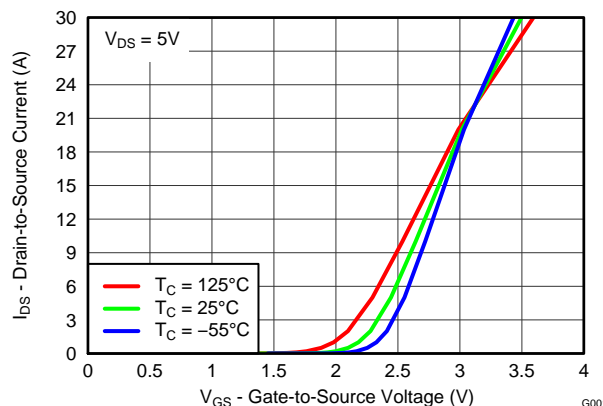


Figure 3. Transfer Characteristics

## TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$  unless otherwise specified

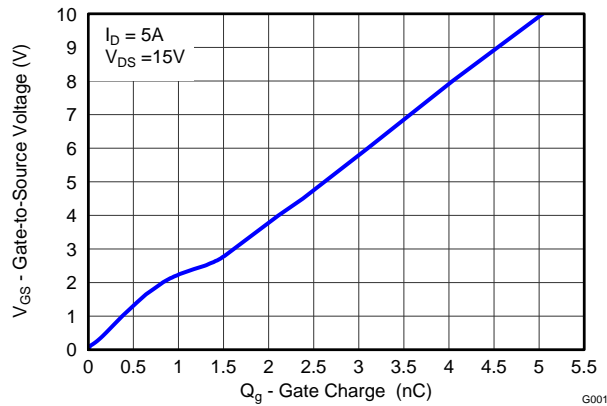


Figure 4. Gate Charge

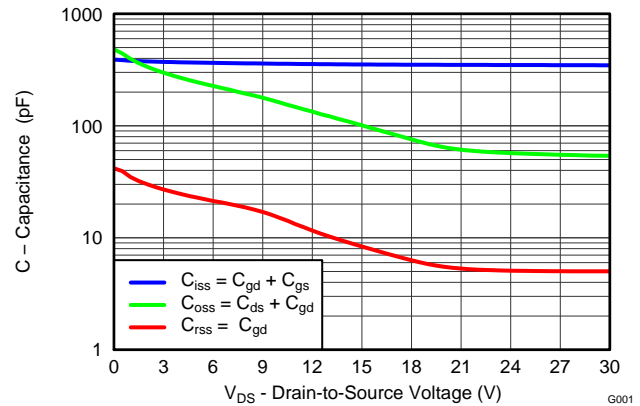


Figure 5. Capacitance

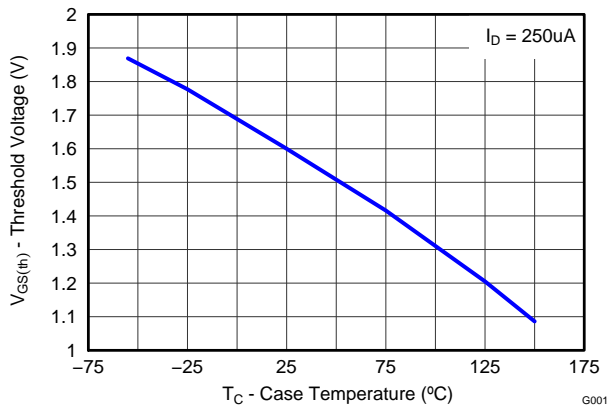


Figure 6. Threshold Voltage vs. Temperature

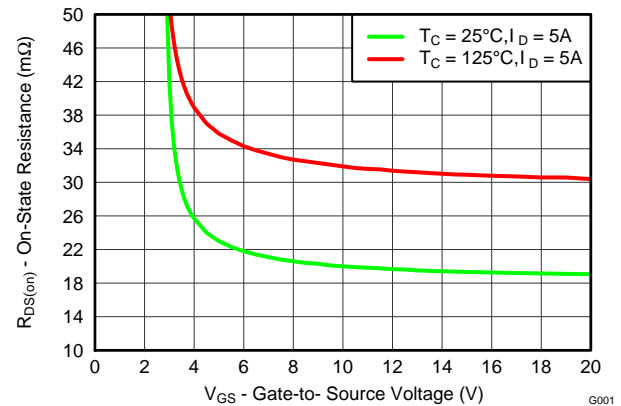


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

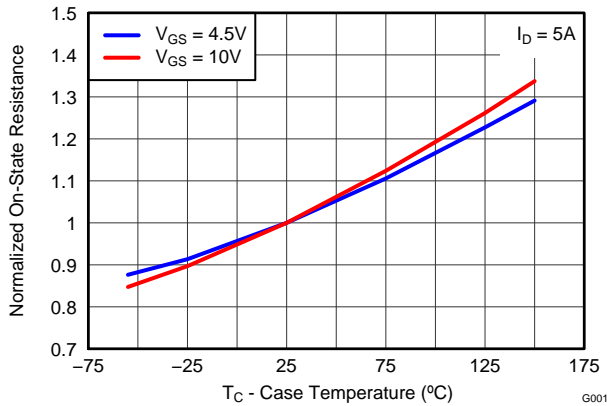


Figure 8. Normalized On-State Resistance vs. Temperature

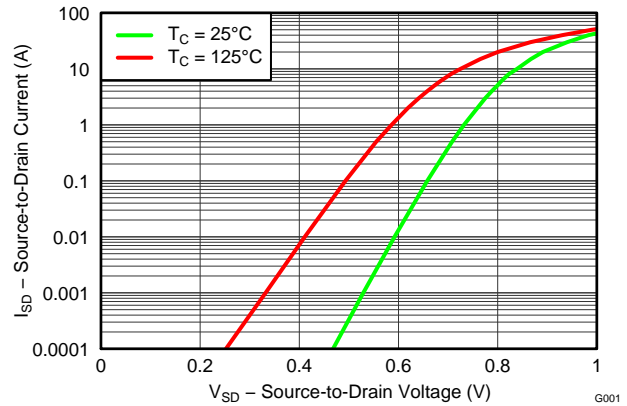
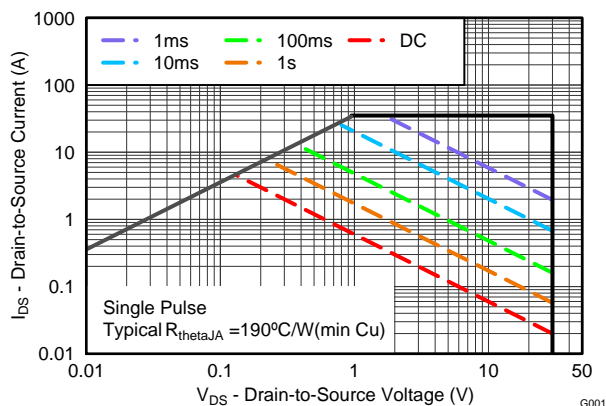


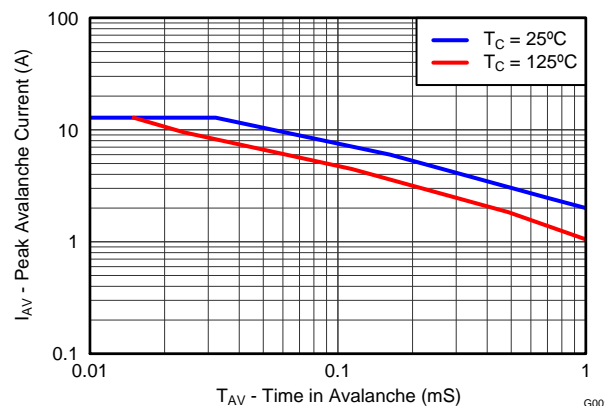
Figure 9. Typical Diode Forward Voltage

## TYPICAL MOSFET CHARACTERISTICS (continued)

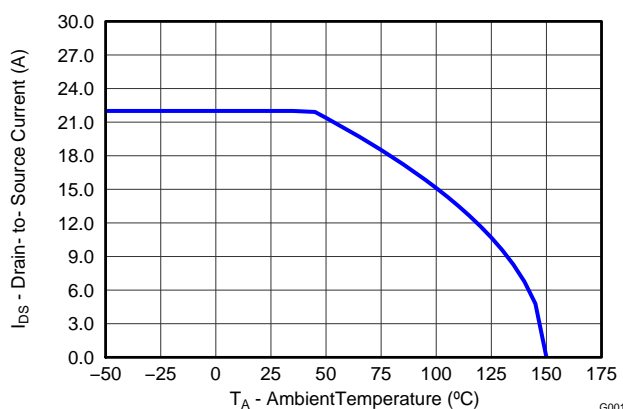
$T_A = 25^\circ\text{C}$  unless otherwise specified



**Figure 10. Maximum Safe Operating Area**



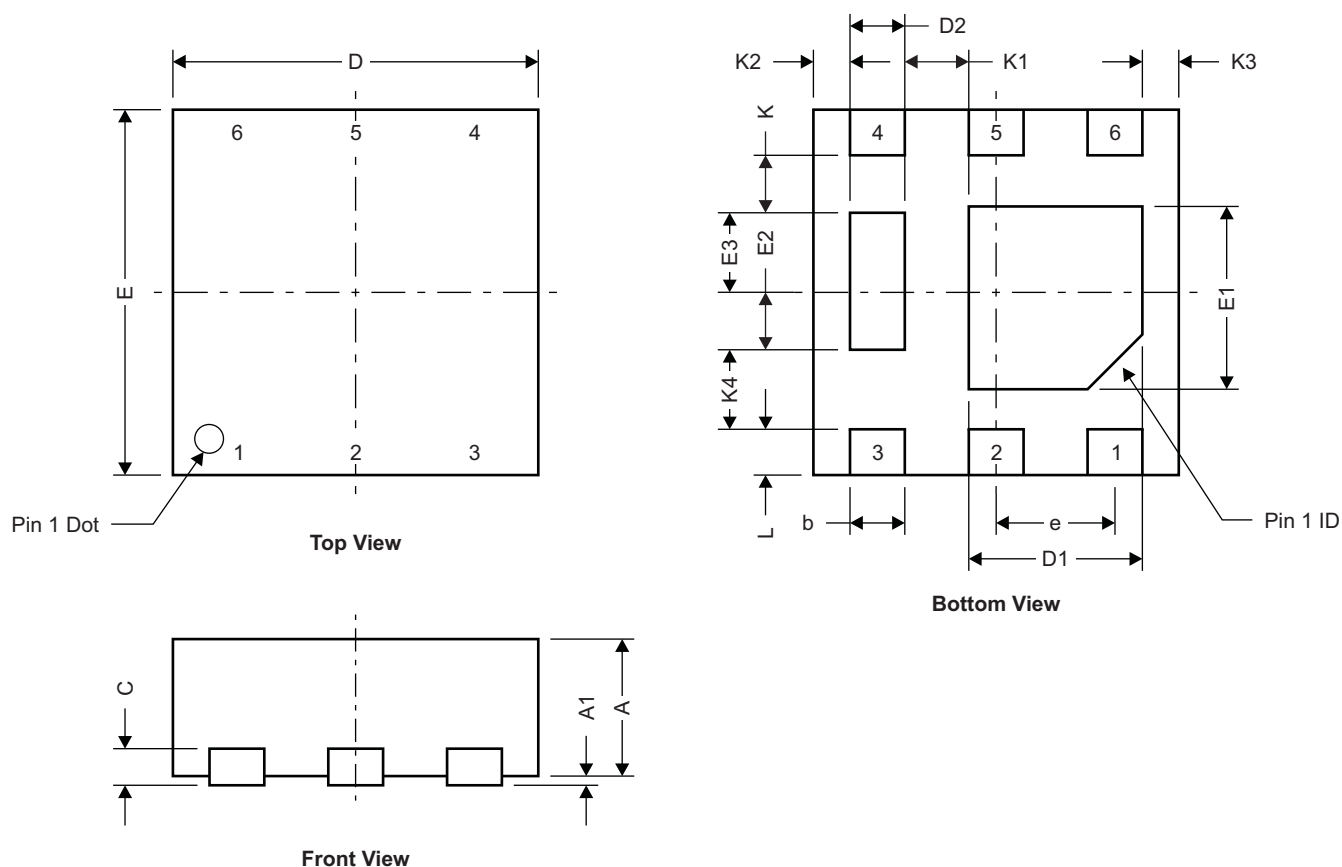
**Figure 11. Single Pulse Unclamped Inductive Switching**



**Figure 12. Maximum Drain Current vs. Temperature**

## MECHANICAL DATA

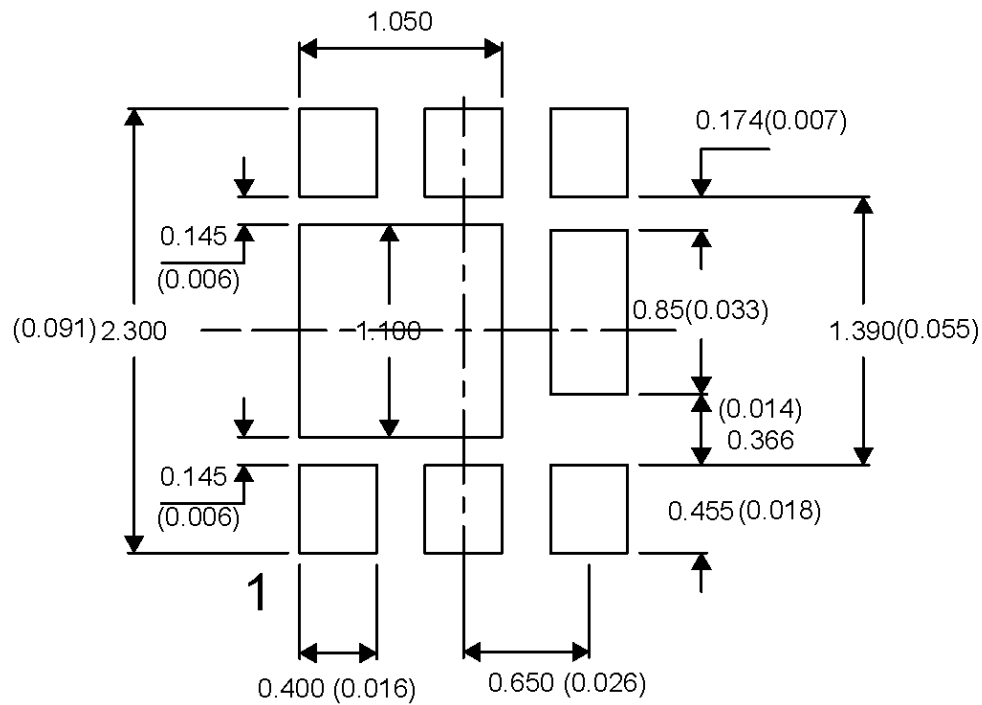
### Q2 Package Dimensions



M0165-01

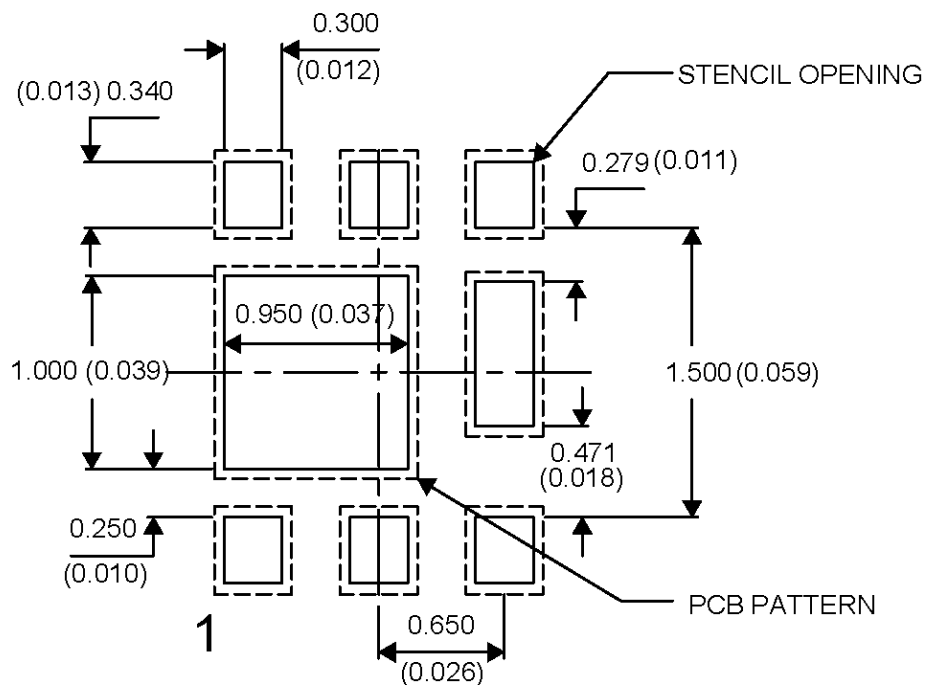
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C	0.203 TYP			0.008 TYP		
D	2.000 TYP			0.080 TYP		
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2	0.300 TYP			0.012 TYP		
E	2.000 TYP			0.080 TYP		
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2	0.280 TYP			0.0112 TYP		
E3	0.470 TYP			0.0188 TYP		
e	0.650 BSC			0.026 TYP		
K	0.280 TYP			0.0112 TYP		
K1	0.350 TYP			0.014 TYP		
K2	0.200 TYP			0.008 TYP		
K3	0.200 TYP			0.008 TYP		
K4	0.470 TYP			0.0188 TYP		
L	0.200	0.25	0.300	0.008	0.010	0.012

## Recommended PCB Pattern



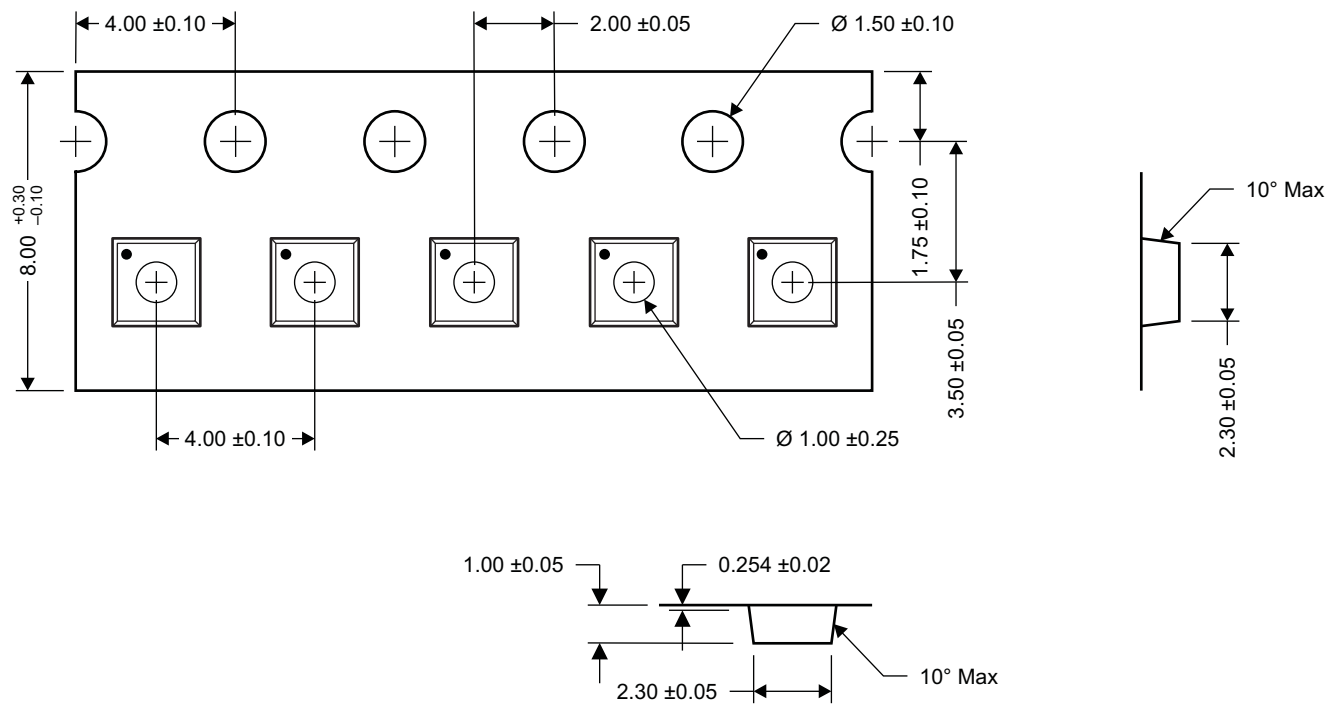
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

### Recommended Stencil Pattern



Note: All dimensions are in mm, unless otherwise specified.

## Q2 Tape and Reel Information



M0168-01

- Notes:
1. Measured from centerline of sprocket hole to centerline of pocket
  2. Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$
  3. Other material available
  4. Typical SR of form tape Max  $10^9$  OHM/SQ
  5. All dimensions are in mm, unless otherwise specified.



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17571Q2	ACTIVE	SON	DQK	6	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 150		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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### Applications

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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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