CM1213A, SZCM1213A

1, 2 and 4-Channel Low Capacitance ESD Protection Arrays

Product Description

The CM1213A family of diode arrays has been designed to provide ESD protection for electronic components or subsystems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N, offering two advantages. First, it protects the V_{CC} rail against ESD strikes, and second, it eliminates the need for a bypass capacitor that would otherwise be needed for absorbing positive ESD strikes to ground. The CM1213A will protect against ESD pulses up to 8 kV per the IEC 61000−4−2 standard.

These devices are particularly well−suited for protecting systems using high−speed ports such as USB 2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD−RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

Features

- One, Two, and Four Channels of ESD Protection
  Note: For 6 and 8−channel Devices, See the CM1213 Datasheet
- Provides ESD Protection to IEC61000−4−2 Level 4
  - ±8 kV Contact Discharge
- Low Channel Input Capacitance of 0.85 pF Typical
- Minimal Capacitance Change with Temperature and Voltage
- Channel Input Capacitance Matching of 0.02 pF Typical is Ideal for Differential Dignals
- Each I/O Pin Can Withstand Over 1000 ESD Strikes*
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

- USB2.0 Ports at 480 Mbps in Desktop PCs, Notebooks and Peripherals
- IEEE1394 Firewire® Ports at 400 Mbps/800 Mbps
- DVI Ports, HDMI Ports in Notebooks, Set Top Boxes, Digital TVs, LCD Displays
- Serial ATA Ports in Desktop PCs and Hard Disk Drives
- PCI Express Ports
- General Purpose High−Speed Data Line ESD Protection

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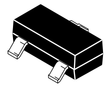
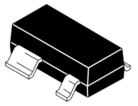
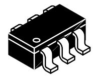


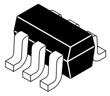
SOT23−3
SO SUFFIX
CASE 318



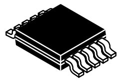
SOT−143
SR SUFFIX
CASE 318A



SC−74
SO SUFFIX
CASE 318F

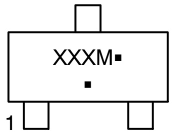


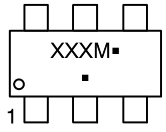
SC70−6
S7 SUFFIX
CASE 419AD



MSOP−10
MR SUFFIX
CASE 846AE

MARKING DIAGRAM





XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
CM1213A−01SO, SZCM1213A−01SO	SOT23−3 (Pb−Free)	3,000 / Tape & Reel
CM1213A−02SR, SZCM1213A−02SR	SOT143−4 (Pb−Free)	3,000 / Tape & Reel
CM1213A−02SO	SC−74 (Pb−Free)	3,000 / Tape & Reel
CM1213A−04S7	SC70−6 (Pb−Free)	3,000 / Tape & Reel
CM1213A−04MR	MSOP−10 (Pb−Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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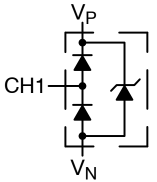
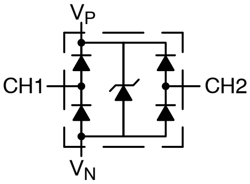
*Standard test condition is IEC61000−4−2 level 4 test circuit with each pin subjected to ±8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

October, 2016 − Rev. 11

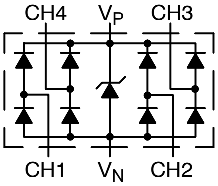
BLOCK DIAGRAM



CM1213A−01SO



CM1213A−02SR
CM1213A−02SO



CM1213A−04MR
CM1213A−04S7

Table 1. PIN DESCRIPTIONS

1–Channel, 3–Lead SOT23–3 Package (CM1213A–01SO)			
Pin	**Name**	**Type**	**Description**
1	CH1	I/O	ESD Channel
2	V_P	PWR	Positive Voltage Supply Rail
3	V_N	GND	Negative Voltage Supply Rail

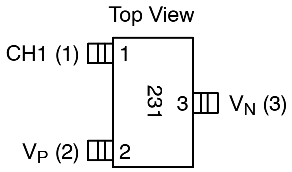
2–Channel, 4–Lead SOT143–4 Package (CM1213A–02SR)			
Pin	**Name**	**Type**	**Description**
1	V_N	GND	Negative Voltage Supply Rail
2	CH1	I/O	ESD Channel
3	CH2	I/O	ESD Channel
4	V_P	PWR	Positive Voltage Supply Rail

2–Channel, SC–74 Package (CM1213A–02SO)			
Pin	**Name**	**Type**	**Description**
1	NC	–	No Connect
2	VN	GND	Negative Voltage Supply Rail
3	CH1	I/O	ESD Channel
4	CH2	I/O	ESD Channel
5	NC	–	No Connect
6	VP	PWR	Positive Voltage Supply Rail

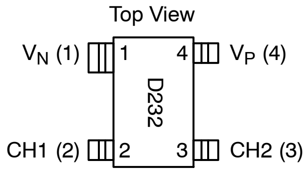
4–Channel, 6–Lead SC70–6 (CM1213A–04S7)			
Pin	**Name**	**Type**	**Description**
1	CH1	I/O	ESD Channel
2	V_N	GND	Negative Voltage Supply Rail
3	CH2	I/O	ESD Channel
4	CH3	I/O	ESD Channel
5	V_P	PWR	Positive Voltage Supply Rail
6	CH4	I/O	ESD Channel

4–Channel, 10–Lead MSOP–10 Package (CM1213A04MR)			
Pin	**Name**	**Type**	**Description**
1	CH1	I/O	ESD Channel
2	NC	–	No Connect
3	V_P	PWR	Positive Voltage Supply Rail
4	CH2	I/O	ESD Channel
5	NC	–	No Connect
6	CH3	I/O	ESD Channel
7	NC	–	No Connect
8	V_N	GND	Negative Voltage Supply Rail
9	CH4	I/O	ESD Channel
10	NC	–	No Connect

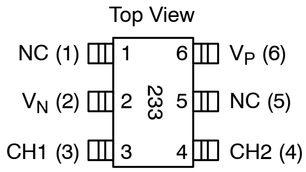
PACKAGE/PINOUT DIAGRAMS



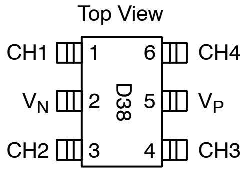
3–Lead SOT23–3



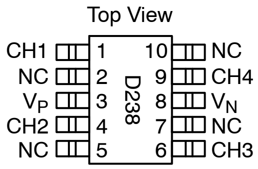
4–Lead SOT143–4



6–Lead SC–74



6–Lead SC70–6



10–Lead MSOP–10

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Supply Voltage (V_P – V_N)	6.0	V
Operating Temperature Range	–40 to +85	°C
Storage Temperature Range	–65 to +150	°C
DC Voltage at any channel input	(V_N – 0.5) to (V_P + 0.5)	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Operating Temperature Range	–40 to +85	°C
Package Power Rating SOT23–3, SOT143–4, SC–74, and SC70–6 Packages MSOP–10 Package	 225 400	mW

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_P	Operating Supply Voltage (V_P–V_N)			3.3	5.5	V
I_P	Operating Supply Current	(V_P–V_N) = 3.3 V			8.0	μA
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8 mA; T_A = 25°C	 0.60 0.60	 0.80 0.80	 0.95 0.95	V
I_{LEAK}	Channel Leakage Current	T_A = 25°C; V_P = 5 V, V_N = 0 V		0.1	1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_P = 3.3 V, V_N = 0 V, V_{IN} = 1.65 V (Note 2)		0.85	1.2	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, V_P = 3.3 V, V_N = 0 V, V_{IN} = 1.65 V (Note 2)		0.02		pF
V_{ESD}	ESD Protection – Peak Discharge Voltage at any channel input, in system Contact discharge per IEC 61000–4–2 standard	T_A = 25°C (Notes 2 and 3)	8			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A = 25°C, I_{PP} = 1A, t_P = 8/20 μS (Note 2)		 +10 –1.7		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I_{PP} = 1A, t_P = 8/20 μS Any I/O pin to Ground (Note 2)		 0.9 0.5		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. All parameters specified at T_A = –40°C to +85°C unless otherwise noted.
2. Standard IEC 61000–4–2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330 Ω, V_P = 3.3 V, V_N grounded.
3. These measurements performed with no external capacitor on V_P (V_P floating).

PERFORMANCE INFORMATION

Input Channel Capacitance Performance Curves

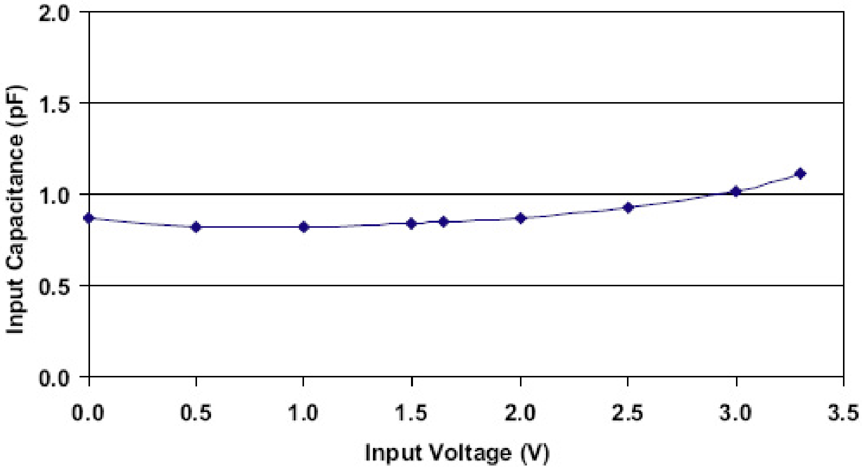


Figure 1. Typical Variation of C_{IN} vs. V_{IN}
(f = 1 MHz, V_P = 3.3 V, V_N = 0 V, 0.1 μF Chip Capacitor between V_P and V_N, 25°C)

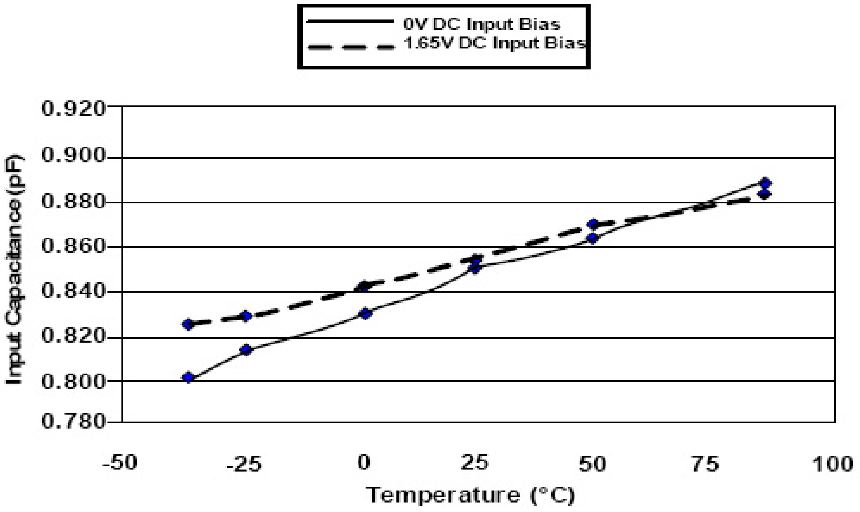


Figure 2. Typical Variation of C_{IN} vs. Temp
(f = 1 MHz, V_{IN} = 30 mV, V_P = 3.3 V, V_N = 0 V, 0.1 μF Chip Capacitor between V_P and V_N)

PERFORMANCE INFORMATION (Cont’d)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

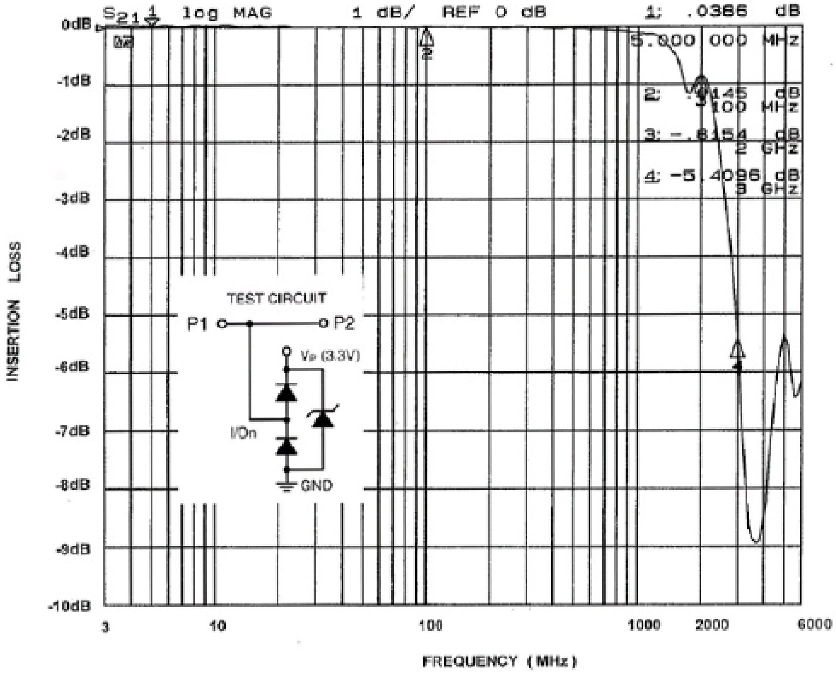


Figure 3. Insertion Loss (S21) vs. Frequency (0 V DC Bias, V_P=3.3 V)

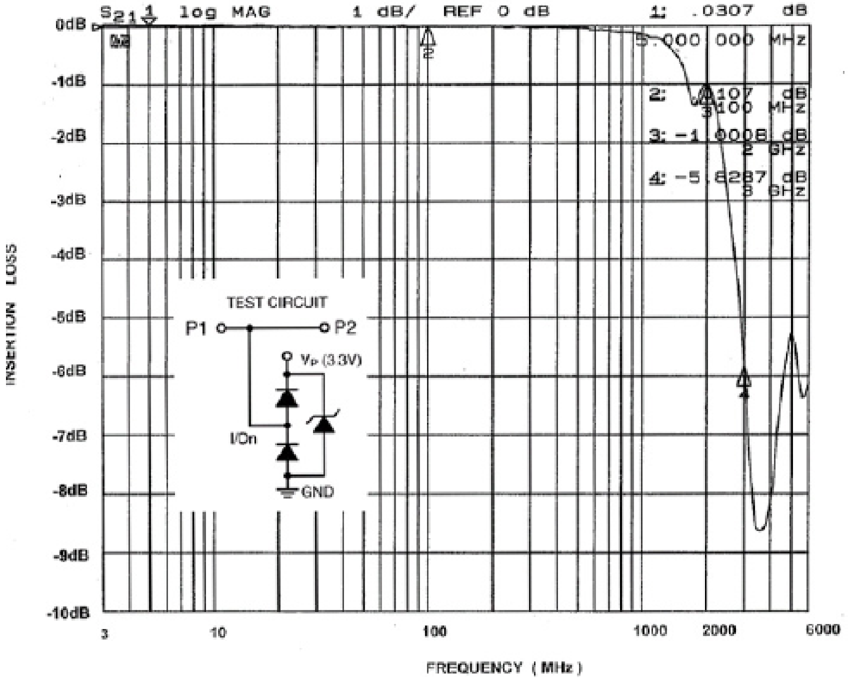


Figure 4. Insertion Loss (S21) vs. Frequency (2.5 V DC Bias, V_P=3.3 V)

APPLICATION INFORMATION

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Application of Positive ESD Pulse between Input Channel and Ground, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2. The voltage V_{CL} on the line being protected is:

$$\mathbf{V_{CL} = Fwd\ Voltage\ Drop\ of\ D_1 + V_{SUPPLY} + L_1\ x\ d(I_{ESD}) / dt + L_2\ x\ d(I_{ESD}) / dt}$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000−4−2 standard results in a current pulse that rises from zero to 30 Amps in 1 ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1x10^{-9})$. So just 10 nH of series inductance (L_1 and L_2 combined) will lead to a 300 V increment in V_{CL}!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1213A has an integrated Zener diode between V_P and V_N. This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the Zener diode. However, for the lowest possible V_{CL}, especially when V_P is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22 μF ceramic chip capacitor be connected between V_P and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also ON Semiconductor Application Note “Design Considerations for ESD Protection”, in the Applications section.

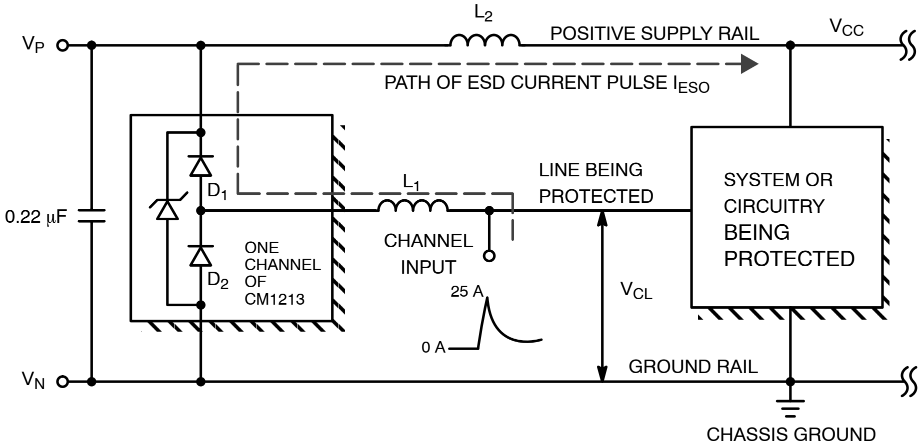
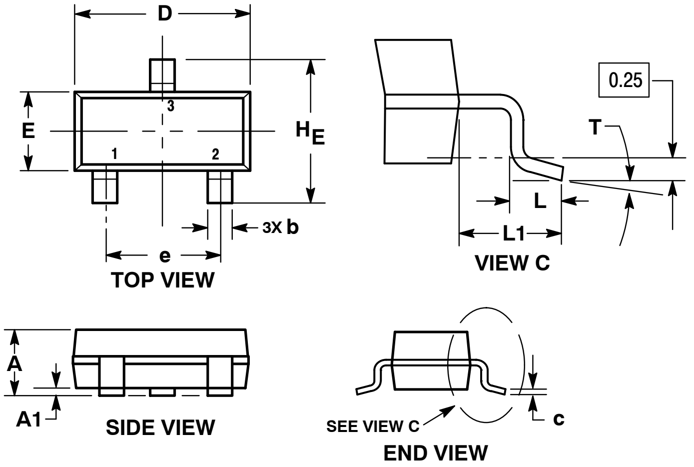


Figure 5. Application of Positive ESD Pulse between Input Channel and Ground

PACKAGE DIMENSIONS

SOT−23 (TO−236)

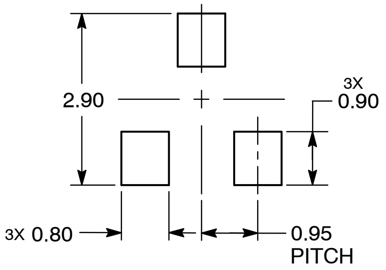
CASE 318−08
ISSUE AR



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	−−−	10 °	0 °	−−−	10 °

RECOMMENDED SOLDERING FOOTPRINT*



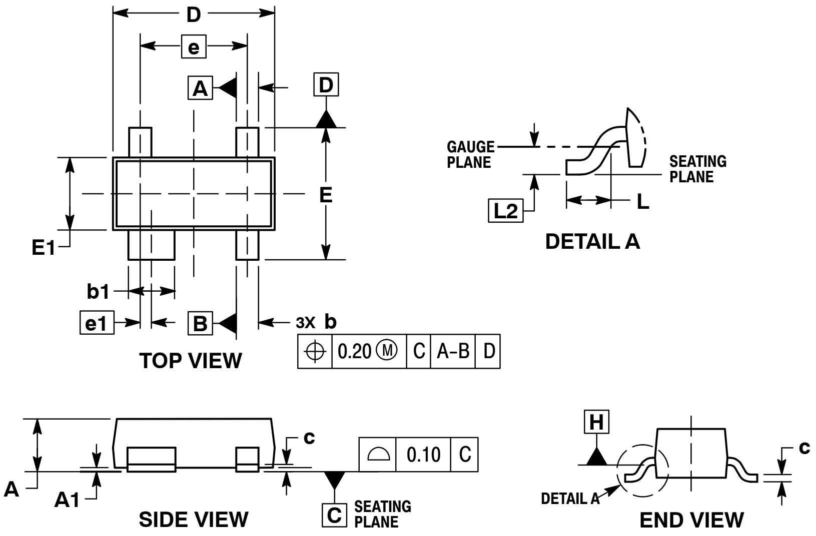
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SOT−143

CASE 318A−06
ISSUE U

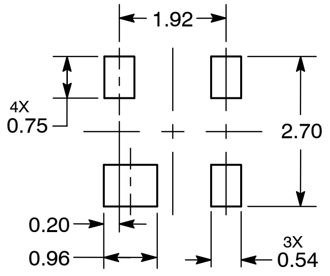


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, AND GATE BURRS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.12
A1	0.01	0.15
b	0.30	0.51
b1	0.76	0.94
c	0.08	0.20
D	2.80	3.05
E	2.10	2.64
E1	1.20	1.40
e	1.92 BSC	
e1	0.20 BSC	
L	0.35	0.70
L2	0.25 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



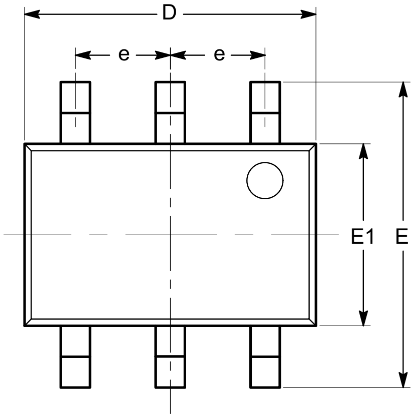
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

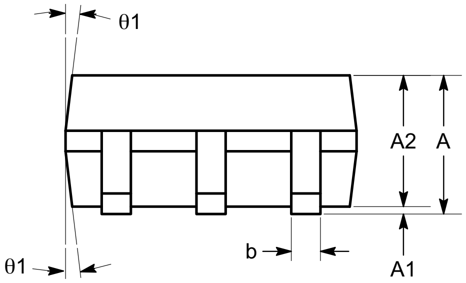
SC−88 (SC−70 6 Lead), 1.25x2

CASE 419AD
ISSUE A

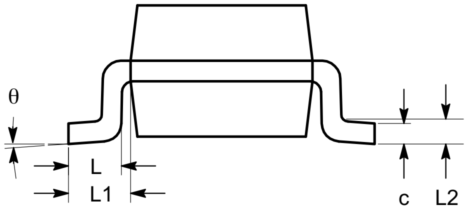


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
θ	0º		8º
θ1	4º		10º



SIDE VIEW



END VIEW

Notes:

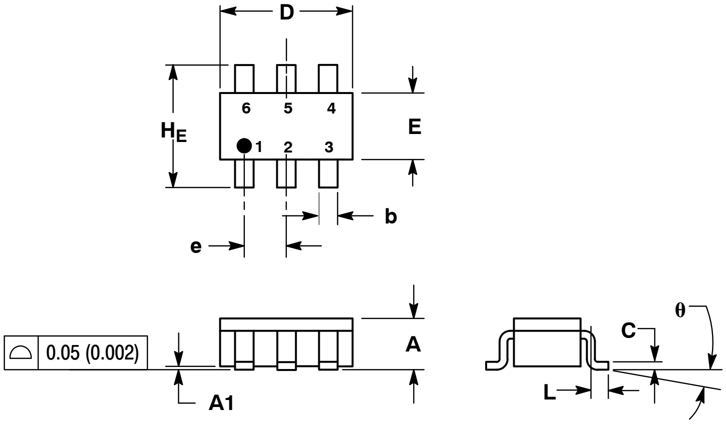
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

PACKAGE DIMENSIONS

SC−74

CASE 318F−05
ISSUE N

SCALE 2:1

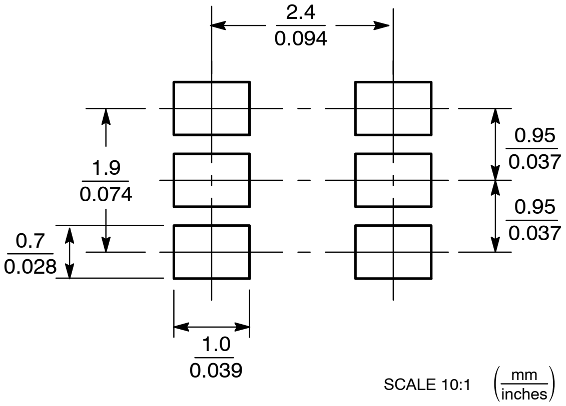


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318F−01, −02, −03, −04 OBSOLETE. NEW STANDARD 318F−05.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.37	0.50	0.010	0.015	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
H_E	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	−	10°	0°	−	10°

SOLDERING FOOTPRINT*

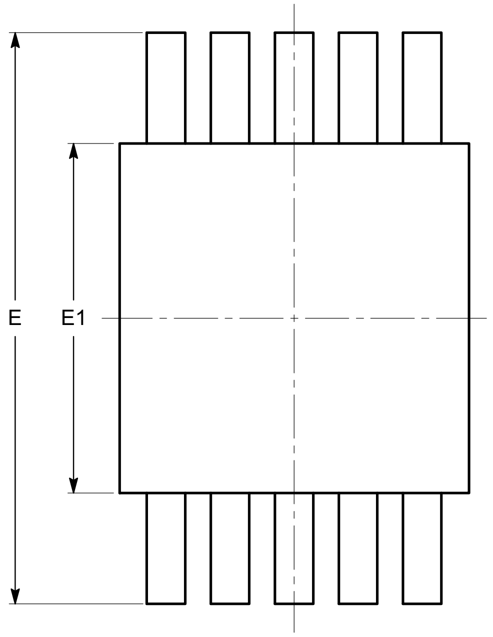


SCALE 10:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

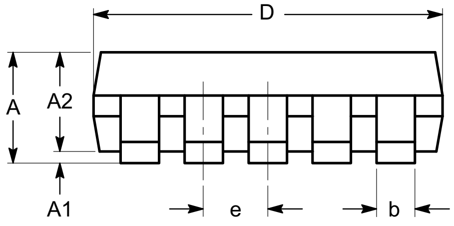
PACKAGE DIMENSIONS

MSOP 10, 3x3
CASE 846AE
ISSUE O

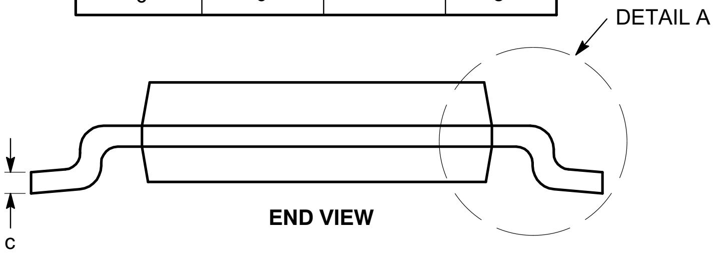


TOP VIEW

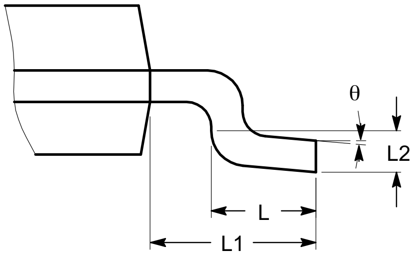
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.00	0.05	0.15
A2	0.75	0.85	0.95
b	0.17		0.27
c	0.13		0.23
D	2.90	3.00	3.10
E	4.75	4.90	5.05
E1	2.90	3.00	3.10
e	0.50 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
θ	0º		8º



SIDE VIEW



END VIEW



DETAIL A

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

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